Data Parallel C++ - New Features

Find out what's new in Data Parallel C++ Language

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LEARNING OBJECTIVES

Use new DPC++ features like Unified Shared Memory to simplify heterogeneous programming

Understand advantages of using Sub-groups in DPC++

Understand advantages of using Data Parallel C++ Library for heterogeneous computing.



WHAT IS DATA PARALLEL C++?

Data Parallel C++

= C++ and SYCL* standard and extensions

Based on modern C++

C++ productivity benefits and familiar constructs

Standards-based, cross-architecture

 Incorporates the SYCL standard for data parallelism and heterogeneous programming



DPC++ EXTENDS SYCL 1.2.1

Enhance Productivity

- Simple things should be simple to express
- Reduce verbosity and programmer burden

Enhance Performance

- Give programmers control over program execution
- Enable hardware-specific features

DPC++: Fast-moving open collaboration feeding into the SYCL* standard

- Open source implementation with goal of upstream LLVM
- DPC++ extensions aim to become core SYCL*, or Khronos* extensions



DPC++ = C++ + SYCL* + NEW FEATURES

DPC++ New Features:

- Unified Shared Memory (USM)
- Sub-Groups
- And more...

Main goals of DPC++ New Features are to simplify programming and achieve performance by exposing hardware features.



UNIFIED SHARED MEMORY (USM)

Unified Shared Memory is <u>pointer-based approach</u> to memory model for heterogeneous programming



WHY UNIFIED SHARED MEMORY (USM)

The SYCL 1.2.1 standard provides a Buffer memory abstraction

- Powerful and elegantly expresses data dependences
 However...
- Replacing all pointers and arrays with buffers in a C++ program can be a burden to programmers

USM provides a pointer-based alternative in DPC++

- Simplifies porting to an accelerator
- Gives programmers the desired level of control
- Complementary to buffers



DEVELOPER VIEW OF USM

Developers can reference same memory object in host and device code with Unified Shared Memory





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DPC++ UNIFIED SHARED MEMORY

Unified Shared Memory enables the accessing memory on the host and device with same pointer reference





SYCL BUFFERS AND ACCESSORS

Memory Model with Buffers & Accessors – requires defining buffers and accessors and synchronize as required



DPC++ UNIFIED SHARED MEMORY

Unified Shared Memory can be setup as follows:

int *data = malloc_shared<int>(N, q);

You can also use a more familiar C++/C style malloc:

int *data = static_cast<int*>(malloc_shared(N * sizeof(int), q));

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DPC++ UNIFIED SHARED MEMORY

Unified shared memory provides both explicit and implicit models for managing memory.

Allocation Type	Description	Accessible on HOST	Accessible on DEVICE
device	Allocations in device memory (explicit)	NO	YES
host	Allocations in host memory (implicit)	YES	YES
shared	Allocations can migrate between host and device memory (implicit)	YES	YES

Automatic data accessibility and explicit data movement supported



USM – EXPLICIT DATA TRANSFER

malloc_device() will allocate memory on device, Host will not have access

Copy memory explicitly from host to device using q.memcpy()

Make any data modification on device

Copy the memory explicitly from device to host using q.memcpy()

Optimization Notice Copyright © 2019, Intel Corporation. All rights reserved. *Other names and brands may be claimed as the property of others. queue q; int *data = static_cast<int*>(malloc(N * sizeof(int))); int *data_device = static_cast<int*>(malloc_device(N * sizeof(int), q)); for(int i=0;i<N;i++) {data[i] = 10;}</pre>

```
auto e1 = q.memcpy(data_device, data, sizeof(int)*N);
auto e2 = q.submit([&] (handler &h){
    h.depends on(e1);
    h.parallel for(range<1>(N), [=](id<1> i){
        data_device[i] *= 2;
    });
});
q.submit([&] (handler &h){
    h.depends on(e2);
    h.memcpy(data, data_device, sizeof(int)*N);
}).wait();
for(int i=0;i<N;i++) std::cout << data[i] << " ";</pre>
free(data); free(data_device, q);
```

USM – IMPLICIT DATA TRANSFER

malloc_shared() will allocate memory that can move between host and device. Host and device will have access

Host has access to the device – modified memory



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USM Implicit and Explicit Data Movement



UNIFIED SHARED MEMORY – WHEN TO USE IT

SYCL* Buffers are powerful and elegant

• Use if the abstraction applies cleanly in your application, and/or buffers aren't disruptive to your development

USM provides a familiar pointer-based C++ interface

- Useful when porting C++ code to DPC++, by minimizing changes
- Use shared allocations when porting code, to get functional quickly
- Note that shared allocation is **not intended** to provide peak performance out of box
- Use explicit USM allocations when controlled data movement is needed



UNIFIED SHARED MEMORY

• Summary

- What is Unified Shared Memory (USM)?
- Implicit and Explicit data movement between host and device
- Handling data dependency in multiple kernel tasks using wait event, depends_on method and in_order queue property





On many modern hardware platforms, a subset of the work-items in a work-group are executed simultaneously or with additional scheduling guarantees.

These subset of work-items are called sub-groups, leveraging sub-groups will help to map execution to lowlevel hardware and may help in achieving higher performance.



ND_RANGE KERNELS

ND-Range kernel is a way to express parallelism which enable mapping executions to compute units on hardware.

range<3> N(8, 8, 8); range<3> B(4, 4, 4);

h.parallel_for(nd_range<3>(N, B), [=](nd_item<1> item){
 // CODE THAT RUNS ON DEVICE

});





HOW IT MAPS TO HARDWARE (INTEL GEN11 GRAPHICS)



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A subset of work-groups called **sub-groups** are mapped to vector hardware





20

A subset of work-items within a work-group that may map to vector hardware.

Why use Sub-groups?

- Work-items in a sub-group can communicate directly using ulletshuffle operations, without explicit memory operations.
- Work-items in a sub-group can synchronize using sub-group \bullet barriers and guarantee memory consistency using sub-group memory fences.
- Work-items in a sub-group have access to sub-group ulletcollectives, providing fast implementations of common parallel patterns.





ND_RANGE KERNEL EXECUTION

Parallel execution with ND_RANGE Kernel helps to group work items that maps to hardware resources. This helps to tune applications for performance.



22

sub_group class

The sub-group handle can be obtained from the nd_item using the get_sub_group()

Once you have the sub-group handle, you can **query** for more information about the sub-group, do shuffle operations or use collective functions. h.parallel_for(nd_range<1>(N,B), [=](nd_item<1> item){

intel::sub_group sg = item.get_sub_group();

// KERNEL CODE

});



});

The sub-group handle can be queried to get other information:

- get_local_id() returns the index of the work-item within its sub-group
- **get_local_range()** returns the size of sub_group
- get_group_id() returns the index
 of the sub-group
- get_group_range() returns the number of sub-groups within the parent work-group

h.parallel_for(nd_range<1>(N,B), [=](nd_item<1> item){
 intel::sub_group sg = item.get_sub_group();

sub_group id: 1 of 4, size=16
sub_group id: 3 of 4, size=16
sub_group id: 2 of 4, size=16
sub_group id: 0 of 4, size=16



});

Sub-Group Shuffles

- One of the most useful features of sub-groups is the ability to communicate directly between individual work-items without explicit memory operations.
- Shuffle operations enable us to remove work-group local memory usage from our kernels and/or to avoid unnecessary repeated accesses to global memory.

```
h.parallel_for(nd_range<1>(N,B), [=](nd_item<1> item){
    intel::sub_group sg = item.get_sub_group();
    size_t i = item.get_global_id(0);
```

```
/* Shuffles */
//data[i] = sg.shuffle(data[i], 2);
//data[i] = sg.shuffle_up(0, data[i], 1);
//data[i] = sg.shuffle_down(data[i], 0, 1);
data[i] = sg.shuffle_xor(data[i], 1);
```





Sub-Group Collectives

- The collective functions provide implementations of closely-related common parallel patterns.
- Providing these implementations as library functions increases developer productivity and gives implementations the ability to generate highly optimized code for individual target devices.

h.parallel_for(nd_range<1>(N,B), [=](nd_item<1> item){
 intel::sub_group sg = item.get_sub_group();

```
size_t i = item.get_global_id(0);
```

```
/* Collectives */
```

data[i] = reduce(sg, data[i], intel::plus<>());

//data[i] = reduce(sg, data[i], intel::maximum<>());

//data[i] = reduce(sg, data[i], inte::minimum<>());

});



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Sub-Group Shuffle and Collectives



• Summary

- What are Sub-Groups?
- Why are they useful?
- Learned about sub-group shuffle operations and using subgroup collectives



WHAT IS DPC++ LIBRARY?

The Intel[®] oneAPI Data Parallel C++ Library (oneDPL) is a companion to the Intel[®] oneAPI DPC++ Compiler and provides an alternative for C++ developers who create heterogeneous applications and solutions.

Its APIs are based on familiar standards and maximizes productivity and performance across CPUs, GPUs, and FPGAs.



WHAT IS DPC++ LIBRARY?

DPC++ Library consists of the following components:

- Standard C++ APIs C++ standard APIs have been tested and function well within <u>DPC++ kernels</u>.
- Parallel STL algorithms which offers efficient support for both parallel and vectorized execution of algorithms for Intel[®] processors is extended with <u>support for DPC++ compliant devices</u> by introducing special DPC++ execution policies.
- Extensions APIs additional set of algorithm, classes and iterators.



WHY USE DPC++ LIBRARY ?

std::sort(oneapi::dpl::execution::make_device_policy(q)),

The Intel oneAPI DPC++ Library helps to maximize productivity and performance across CPUs, GPUs, and FPGAs.

Compute on host

> std::sort(v.begin(), v.end());

Compute on GPU with oneDPL

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queue q(gpu selector{});

);

Execution policy tells where the library function is executed

v.begin(), v.end()



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WHY USE DPC++ LIBRARY ?

Lets look at a simple DPC++ code example and see how DPC++ Library can be used to simplify programming.

queue q; std::vector<int> v(N); { DPC++ Kernel buffer<int> buf(v.data(),v.size()); Code can be q.submit([&](handler &h){ auto V = buf.get_access<access::mode::read_write>(h); accomplished with h.parallel_for(range<1>(N),[=] (id<1> i){ V[i] = 20; }); one line of }); oneDPL code }

for(int i = 0; i < v.size(); i++) std::cout << v[i] << std::endl;</pre>

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32

WHY USE DPC++ LIBRARY ?

The DPC++ library function used here is Parallel STL std::fill, which executes the functionality on the device and handles all the memory transfers.

	<pre>queue q; std::vector<int> v(N);</int></pre>
DPC++ Library function	<pre>std::fill(oneapi::dpl::execution::make_device_policy(q), v.begin(), v.end(), 20);</pre>
	<pre>for(int i = 0; i < v.size(); i++) std::cout << v[i] << std::endl;</pre>



DPC++ LIBRARY EXAMPLE

Familiar Parallel STL standard algorithm with a execution policy that executes on heterogeneous device and is optimized for data parallelism.



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HOW DPC++ LIBRARY WORKS?

- Parallel STL algorithms can be called with ordinary iterators
- A temporary SYCL buffer is created and the data is copied to this buffer.
- After processing of the temporary buffer on a device is complete, the data is copied back to the host.

std::fill(oneapi::dpl::execution::make_device_policy(q), v.begin(), v.end(), 20);

MULTIPLE DPC++ LIBRARY ALGORITHMS

Lets look at a simple DPC++ code example that uses multiple oneDPL algorithms

queue q;

```
std::vector<int> v{2,3,1,4};
```

Works **but** memory is copied back to host after each library function

```
std::for_each(make_device_policy(q), v.begin(), v.end(), [](int &a){ a *= 2; });
```

```
std::sort(make_device_policy(q), v.begin(), v.end());
```

for(int i = 0; i < v.size(); i++) std::cout << v[i] << std::endl;</pre>

To minimize copies and retain memory on device, we use "Buffer Iterators"



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DPC++ LIBRARY – BUFFER ITERATORS

Lets look at a how we can minimize memory copies by using buffer iterators





DPC++ LIBRARY – USM POINTERS

Lets look at a simple DPC++ code example and see how DPC++ Library can be used with Unified Shared Memory (USM) pointers.





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oneAPI Data Parallel C++ Library





DPC++ is a standards-based, cross-architecture language to deliver uncompromised productivity and performance across CPUs and accelerators

Extends the SYCL 1.2.1 standard with new features •

New features being developed through a community project

- https://github.com/intel/llvm ullet
- Feel free to open an Issue or submit a PR! ullet



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