



IXPUG Workshop HPC Asia 2021

Welcome Note

Taisuke Boku (CCS, University of Tsukuba)
& Toshihiro Hanawa (ITC, the University of Tokyo)

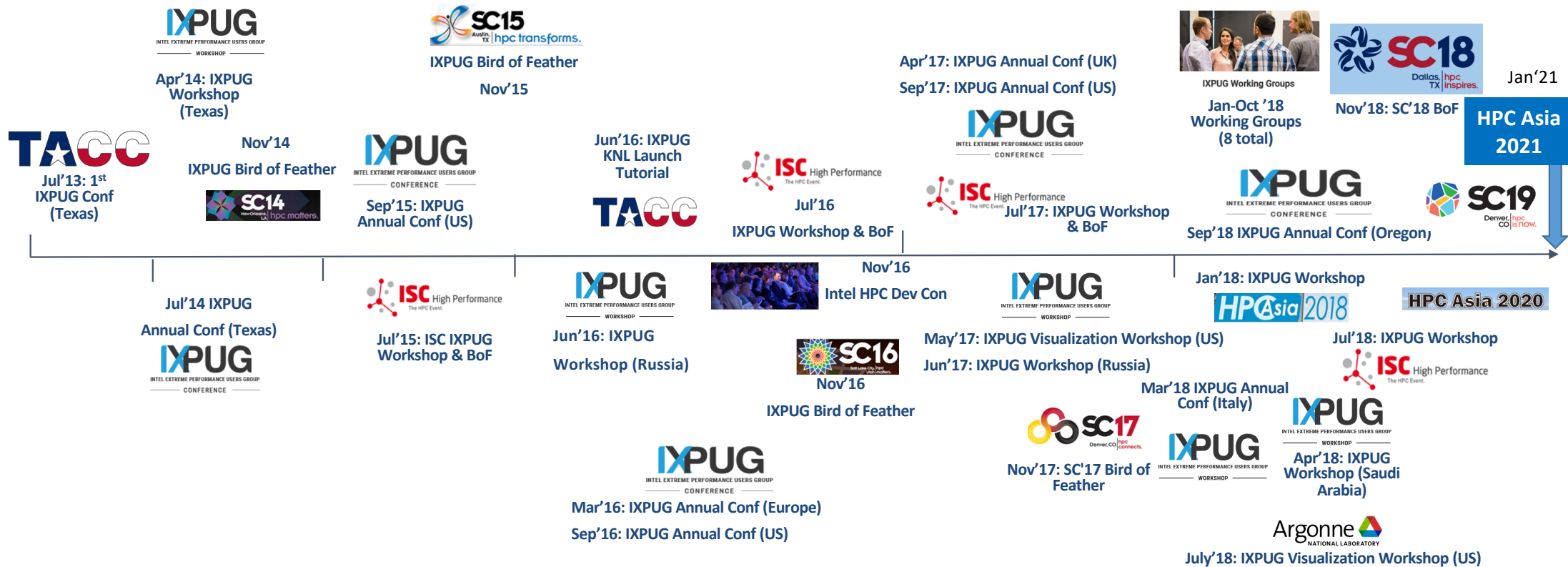
Workshop Organizing Co-Chairs

About IXPUG

IXPUG = Intel eXtreme Performance Users Group

- Independent users group
- Provide a forum for the free exchange of information
- Enhancing the usability and efficiency of HPC & AI/DL workloads
- Computing systems using Intel® architecture
- Fosters technical collaboration...
 - ❖ System architecture beyond the processor (memory, interconnect)
 - ❖ Software tools and programming models
 - ❖ New workloads (HPC, data analytics, AI, visualization, etc.)
- Freely exchanging best practices, experiences worldwide (open to the public)
- Strong technical support from Intel experts

IXPUG Event Momentum



40+ events; 380+ publications; 600+ members

All technical presentations and recordings are posted on www.ixpug.org

January 21, 2021

How to Get Involved

Join, Engage and Share:

- Connect with us on Twitter [@IXPUG1](#)
- Become a member and encourage others to join, by registering at www.ixpug.org
- Contribute by sharing your learnings and experiences in using Intel technology in the regular **IXPUG Webinar** series
- Attend an IXPUG Conferences, Workshops, Birds-of-Feather, Webinar, etc.
- Post a question, share a technique, best practices, etc. on the “Discussion” board at <https://www.ixpug.org/discussion>

Additional Opportunities:

- **Join the IXPUG Steering Committee**
- Questions: → info@ixpug.org

IXPUG Steering Committee

Leadership Board



President

Thomas Steinke
Zuse Institute Berlin



Vice-President

R. Glenn Brook
University of Tennessee Knoxville



Secretary

Melyssa Fratkin
Texas Advanced Computing Center
The University of Texas at Austin

IXPUG Steering Committee



Taisuke Boku
University of Tsukuba



Richard Gerber
NERSC/Lawrence Berkeley
National Laboratory



Clay Hughes
Sandia National
Laboratory



David Keyes
King Abdullah University of
Science & Technology



Nalini Kumar
Intel Corporation



James Lin
Shanghai Jiao Tong University



David Martin
Argonne National Laboratory



Maria Girone
CERN openlab



Vladimir Mironov
Lomonosov Moscow State
University



Sergi Siso
UK Science & Technology
Facilities Council

January 21, 2021

How to Achieve Performance on Current and Future Large Intel-based Systems?

IXPUG community has...

- in-depth knowledge and experience preparing codes for Intel Xeon Phi and Xeon Scalable family of processors and coprocessors

Now and the future:

- FPGA with large LE and high speed interconnect
- In 2021, exascale system with Intel GPUs will be installed
- IXPUG's optimization targets will be expanding: CPU, GPU, FPGA

Challenges on Heterogeneous Architectures

- Technology development and power demands
→ heterogeneity with a larger technology zoo:
 - ❖ Processing data: CPU, GPU, FPGA, AI
 - ❖ Storing data: ..., HBM, ... , NVRAM (DCPMM), SSDs, ...
- Programmability / Productivity
 - ❖ Programming models, languages, ..., standards
- Performance vs. Portability
 - ❖ Expectations for performance portability, if any?
- Software maintenance → Programming Framework

Workshop Program

- Keynote and Invited talks
 - ❖ Advancing HPC Together
John K. Lee (Intel)
 - ❖ oneAPI Industry Initiative for Accelerated Computing
Joe Curley (Intel)
- Five contributed papers (papers available on ACM digital library)
 - ❖ 4 Full Papers
 - ❖ 1 Short Paper
- All presentation video and slides will be on IXPUG website
- Break (10:55-11:15)

ENJOY!