## DISTRIBUTED TENSORFLOW\* TRAINING WITH INTEL® NGRAPH LIBRARY ON INTEL® XEON® SCALABLE PROCESSORS

Jianying Lang, Deep Learning Engineer Artificial Intelligence Products Group Data Center Group Intel Corporation July 11<sup>th</sup>, 2019

## Outline

- Why and what is nGraph?
- Distributed training architecture on nGraph
- Scaling and convergence results
- Conclusion and next steps



## Why nGraph

https://vimeo.com/347401000

Courtesy to AIPG marketing team

Reduces the optimization complexity from O(m\*n) to O(m+n)



#### nGraph - Open source C++ library, compiler & runtime for DL



Intel nGraph Compiler stack contains trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. \*Other names and brands may be claimed as the property of others; see the <u>branding notice</u> and documentation for further details: <u>https://ngraph.nervanasys.com/docs/latest</u>

(intel)

## nGraph Stack



intel

#### Easy to use

- Easy to install and use
- Support both training and inference
- Performance is on par or better than the direct optimization
- Minimize the changes from the user side
  - -Take Tensorflow as an example -Users only need to add the following in their script import ngraph\_bridge



TensorFlow Graph: Graph Marked for Clustering

## Computing architecture for machine learning tasks

- The ultimate goal is to design a heterogeneous computing system with multiple kinds of processors to gain performance and energy efficiency in handling large-scale machine learning tasks.
- As a first step, we are focusing on distributed training using one architecture during the runtime.
- One goal is to develop generic distributed feature in nGraph which could be easily applied to all the framework platforms without much change from user side.



## Data Parallel on nGraph

Each device will have a replica of the training script (graph)

- The training data is distributed on each device
- Each device runs its own data through the model and computes the local gradient
- Gradients on each device will be averaged though a gather-scattering process (allreduce)

The model will be updated with the averaged gradients



## Synchronous SGD



## Asynchronous SGD



## Horovod<sup>\*</sup> -- MPI

- Horovod<sup>\*</sup> is a distributed training framework for TensorFlow<sup>\*</sup>, Keras<sup>\*</sup>, PyTorch<sup>\*</sup>, and MxNet<sup>\*</sup>.
- It utilize the MPI technique for the communication
- $\bullet$  The installation requires MPI library and then pip install Horovod  $^{\ast}$
- This framework is user friendly and it requires less code change from user side than parameter server does
- Better scaling performance
  - MPI transparently sets up the distributed infrastructure necessary for workers to communicate with each other.
  - The MPI communication coordination implementation reduces the wait time for each device

## Distributed training results

- The distributed model needs to achieve the scaling efficiency from training time to standard top-1/top-5 accuracy and scale up to a large number of nodes.
- The current distributed development in nGraph focuses on main framework: TensorFlow<sup>\*</sup>, PaddlPaddle<sup>\*</sup>, and MxNet<sup>\*</sup>.
- This presentation will only showTensorFlow<sup>\*</sup> results.
- Data parallel is used for distributed training. The batch size per device keeps the same.



## Performance benchmark with Horovod\*

We have achieved good multi-node scaling in nGraph using Horovod<sup>\*</sup> by placing the communication op (AllReduce) on Intel<sup>®</sup> Xeon<sup>®</sup>



- Single node performs better with 2 processes mapped by socket using mpirun
- >96% scaling up to 16 nodes with Ethernet interconnect
- 16 2S Intel<sup>®</sup> Xeon<sup>®</sup> Platinum 8180 CPU nodes RN50 training achieves 15.4x performance gain compared to the single 2S node

#### ResNet-50 with Imagenet 1K dataset using Horovod and nGraph TensorFlow

Performance results are based on testing as of 11/07/2018, and may not reflect all publicly available security updates. See configuration disclosure for details on slide 27. No product can be absolutely secure. Optimization Notice: Intel's compilers may or may not optimize to the same degree for non-Intel microprocessors for optimizations that are not unique to Intel microprocessors. These optimizations include SSE2, SSE3, and SSSE3 instruction sets and other optimizations. Intel does not guarantee the availability, functionality, or effectiveness of any optimization on microprocessors not manufactured by Intel. Microprocessors-dependent optimizations in this product are intended for use with Intel microprocessors. Certain optimizations not specific to Intel microarchitecture are reserved for Intel microprocessors. Please refer to the applicable product User and Reference Guides for more information regarding the specific instruction sets covered by this notice. Software and workloads used in performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more complete information visit: http://www.intel.com/performance

## Convergence test (single node)

Hyper parameter tuning is the key to get convergence to the targeted accuracy for multinode training

Larger batch size requires larger learning rate (lr < Total Batch Size)

Take tf\_cnn\_benchmark model script as an example, the validation accuracy @top-1 is 75.5% and accuracy@top-5 is 92.54% at 90 epochs



Performance results are based on testing as of 10/20/2018, and may not reflect all publicly available security updates. See configuration disclosure for details on slide 27. No product can be absolutely secure. Optimization Notice: Intel's compilers may or may not optimize to the same degree for non-Intel microprocessors for optimizations that are not unique to Intel microprocessors. These optimizations include SSE2, SSE3, and SSSE3 instruction sets and other optimizations. Intel does not guarantee the availability, functionality, or effectiveness of any optimization on microprocessors not manufactured by Intel. Microprocessors-dependent optimizations in this product are intended for use with Intel microprocessors. Certain optimizations not specific to Intel microarchitecture are reserved for Intel microprocessors. Please refer to the applicable product User and Reference Guides for more information regarding the specific instruction sets covered by this notice. Software and workloads used in performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more complete information visit: http://www.intel.com/performance

#### Multi-node convergence for ResNet50 I1K

learning\_rate

0.400

By 90 epochs on 8 2S Intel<sup>®</sup> Xeon<sup>®</sup> Platinum 8180 CPU nodes

•75.5% accuracy@top-1

•92.5% accucary@top-5

By 90 epochs on 16 2S Intel<sup>®</sup> Xeon<sup>®</sup> Platinum 8180 CPU nodes

•75.0% accuracy@top-1

•92.3% accuracy@top-5







Performance results are based on testing as of 11/07/2018, and may not reflect all publicly available security updates. See configuration disclosure for details on slide 27. No product can be absolutely secure. Optimization Notice: Intel's compilers may or may not optimize to the same degree for non-Intel microprocessors for optimizations that are not unique to Intel microprocessors. These optimizations include SSE2, SSE3, and SSE3 instruction sets and other optimizations. Intel does not guarantee the availability, functionality, or effectiveness of any optimization on microprocessors not manufactured by Intel. Microprocessors-dependent optimizations in this product are intended for use with Intel microprocessors. Certain optimizations not specific to Intel microarchitecture are reserved for Intel microprocessors. Please refer to the applicable product User and Reference Guides for more information regarding the specific instruction sets covered by this notice. Software and workloads used in performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more complete information visit: http://www.intel.com/performance

0.000

10.00k

20.00k

30.00k

## Conclusion

- Intel<sup>®</sup> developed open source code nGraph (C++) support distributed training and we have successfully run distributed ResNet50 I1K through nGraph on Intel<sup>®</sup> Xeon<sup>®</sup>.
- On multi-node Intel<sup>®</sup> Xeon<sup>®</sup> nodes , we have achieved the start-of-art ResNet50 accuracy@top-1 and accuracy@top-5.
- The performance reaches >96% of scaling efficiency up to 16 2s Intel<sup>®</sup> Xeon<sup>®</sup> Platinum 8180 CPU nodes.
- Work in progress on scaling nGraph to a large number of cluster nodes and developing model parallel support.



#### **Configuration Details**

Platforms: Intel® Xeon® Platinum 8180 CPU @ 2.50GHz, 2 sockets, 28 cores per socket, Link encap:Ethernet

model repos: https://github.com/tensorflow/models.git

Benchmark scripts: https://github.com/tensorflow/benchmarks.git

Tensorflow framework: https://github.com/tensorflow/tensorflow.git

Ngraph-TF: <a href="https://github.com/NervanaSystems/ngraph-tf.git">https://github.com/NervanaSystems/ngraph-tf.git</a>

Horovod: https://github.com/uber/horovod.git

Run command: export OMP\_NUM\_THREADS=28 export PYTHONPATH=\$PYTHONPATH:<path-to-models>/models

mpirun --mca btl\_tcp\_if\_include eno1 -np 16 -x LD\_LIBRARY\_PATH -H skx123,skx124,skx125,skx126, skx127,nervana-skx128,skx129,skx130 -x OMP\_NUM\_THREADS -x PYTHONPATH -cpus-per-proc 28 -map-by socket --oversubscribe --report-bindings python tf\_cnn\_benchmarks.py --variable\_update horovod --model=official\_resnet50 --batch\_size=128 --data\_format NCHW --num\_intra\_threads 28 --num\_inter\_threads 2 --horovod\_device cpu --nodistortions -num\_epochs=90 --num\_warmup\_batches=3125 --save\_model\_secs=625 --mkl=true --data\_name=imagenet --data\_dir /dataset/TF\_Image Net\_latest/ -train\_dir 8node\_resnet50 --datasets\_use\_prefetch=False --kmp\_blocktime=1 --kmp\_affinity=granularity=fine,compact,1,0 --eval\_interval\_secs=625 -print\_training\_accuracy=True --summary\_verbosity=2 --benchmark\_log\_dir=benchmark\_logs --optimizer=sgd --save\_summaries\_steps=20

mpirun --mca btl\_tcp\_if\_include eno1 -np 32 -x LD\_LIBRARY\_PATH -H skx117, skx118, skx119, skx120, skx121, skx122, skx123, skx124, skx125, skx126, skx127, skx128, skx129, skx130, skx131, skx132 -x OMP\_NUM\_THREADS -x PYTHONPATH -cpus-per-proc 28 -map-by socket --oversubscribe --report-bindings python tf\_cnn\_benchmarks.py --variable\_update horovod --model=official\_resnet50 --batch\_size=128 --data\_format NCHW --num\_intra\_threads 28 --num\_in ter\_threads 2 --horovod\_device cpu --nodistortions --num\_epochs=90 --num\_warmup\_batches=1563 --save\_model\_secs=313 --mkl=true -- data\_name=imagenet --data\_dir /dataset/TF\_ImageNet\_latest/ --train\_dir /mnt/data/langjian/16node\_resnet50\_accu racy\_sgd\_90epoch -- datasets\_use\_prefetch=False --kmp\_blocktime=1 --kmp\_affinity=granularity=fine,compact,1,0 --eval\_interval\_secs=313 --print\_training\_accuracy=True -- summary\_verbosity=2 --benchmark\_log\_dir=benchmark\_logs --optimizer=sgd - \_-save\_summaries\_steps=20

Performance results are based on testing as of 11/07/2018, and may not reflect all publicly available security updates. No product can be absolutely secure. Optimization Notice: Intel's compilers may or may not optimize to the same degree for non-Intel microprocessors for optimizations that are not unique to Intel microprocessors. These optimizations include SSE2, SSE3, and SSSE3 instruction sets and other optimizations. Intel does not guarantee the availability, functionality, or effectiveness of any optimization on microprocessors not manufactured by Intel. Microprocessor-dependent optimizations in this product are intended for use with Intel microprocessors. Certain optimizations not specific to Intel microarchitecture are reserved for Intel microprocessors. Please refer to the applicable product User and Reference Guides for more information regarding the specific instruction sets covered by this notice. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more complete information visit: http://www.intel.com/performance

# **NOTICES AND DISCLAIMERS**

Intel technologies' features and benefits depend on system configuration and may require enabled hardware, software or service activation. Performance varies depending on system configuration.

No computer system can be absolutely secure.

Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more complete information visit <a href="http://www.intel.com/benchmarks">http://www.intel.com/benchmarks</a>.

Intel<sup>®</sup> Advanced Vector Extensions (Intel<sup>®</sup> AVX)\* provides higher throughput to certain processor operations. Due to varying processor power characteristics, utilizing AVX instructions may cause a) some parts to operate at less than the rated frequency and b) some parts with Intel<sup>®</sup> Turbo Boost Technology 2.0 to not achieve any or maximum turbo frequencies. Performance varies depending on hardware, software, and system configuration and you can learn more at <a href="http://www.intel.com/go/turbo">http://www.intel.com/go/turbo</a>.

Intel's compilers may or may not optimize to the same degree for non-Intel microprocessors for optimizations that are not unique to Intel microprocessors. These optimizations include SSE2, SSE3, and SSSE3 instruction sets and other optimizations. Intel does not guarantee the availability, functionality, or effectiveness of any optimization on microprocessors not manufactured by Intel. Microprocessor-dependent optimizations in this product are intended for use with Intel microprocessors. Certain optimizations not specific to Intel microarchitecture are reserved for Intel microprocessors. Please refer to the applicable product User and Reference Guides for more information regarding the specific instruction sets covered by this notice.

Cost reduction scenarios described are intended as examples of how a given Intel-based product, in the specified circumstances and configurations, may affect future costs and provide cost savings. Circumstances will vary. Intel does not guarantee any costs or cost reduction.

Intel does not control or audit third-party benchmark data or the web sites referenced in this document. You should visit the referenced web site and confirm whether referenced data are accurate. Intel, the Intel logo, and Intel Xeon are trademarks of Intel Corporation in the U.S. and/or other countries. \*Other names and brands may be claimed as property of others.

© 2019 Intel Corporation.



