

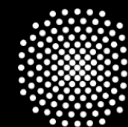
# Screen-Space Normal Distribution Function Caching for Consistent Multi-Resolution Rendering of Large Particle Data ... A CPU Prospect?

**Mohamed Ibrahim**<sup>1</sup>, Patrick Wickenhäuser<sup>2</sup>, Peter Rautek<sup>1</sup>,  
Guido Reina<sup>2</sup>, Markus Hadwiger<sup>1</sup>

<sup>1</sup>King Abdullah University of Science and Technology (KAUST),

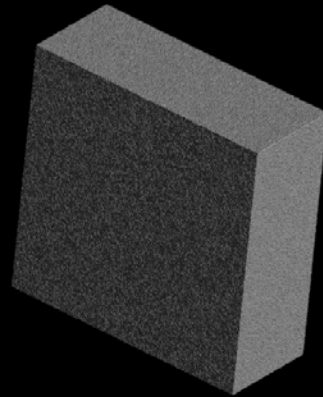
<sup>2</sup>University of Stuttgart

IEEE VIS 2017

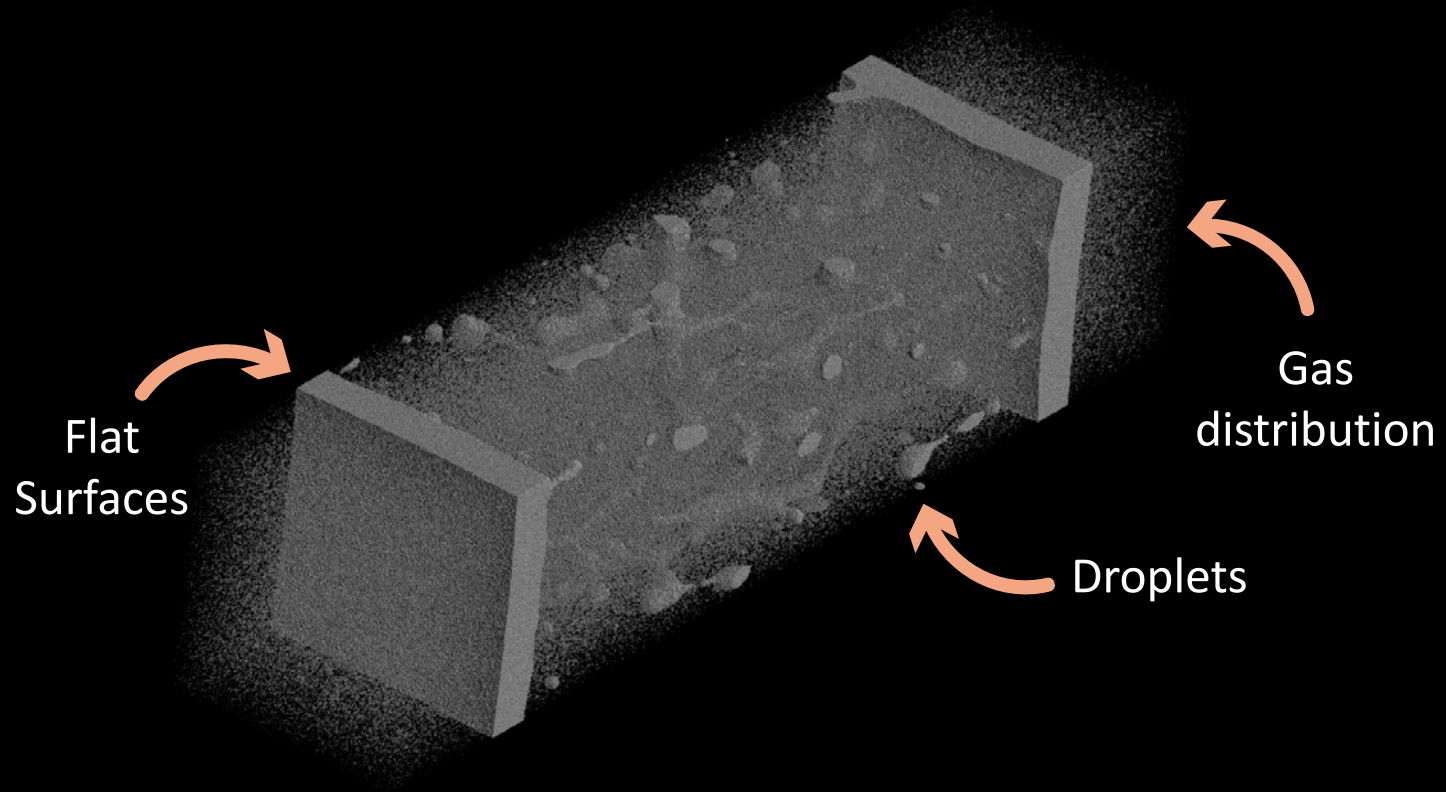


**University of Stuttgart**  
Germany

## Expanding Fluid Layer (30 million particles)

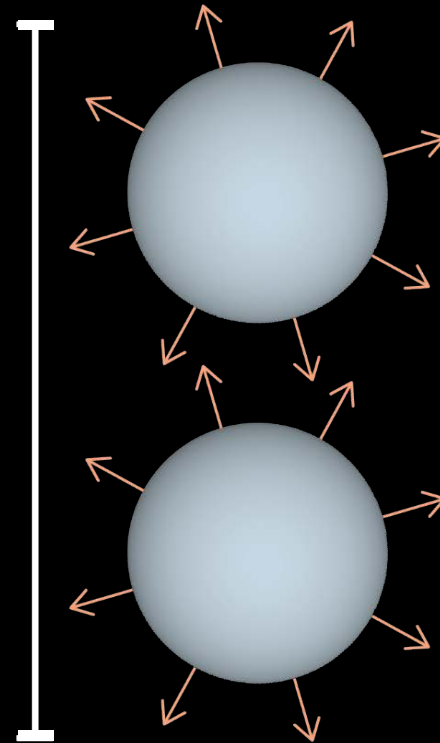
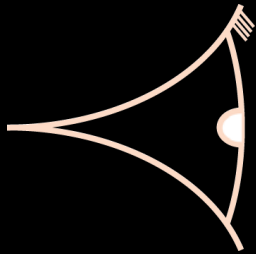


## Expanding Fluid Layer (30 million particles)

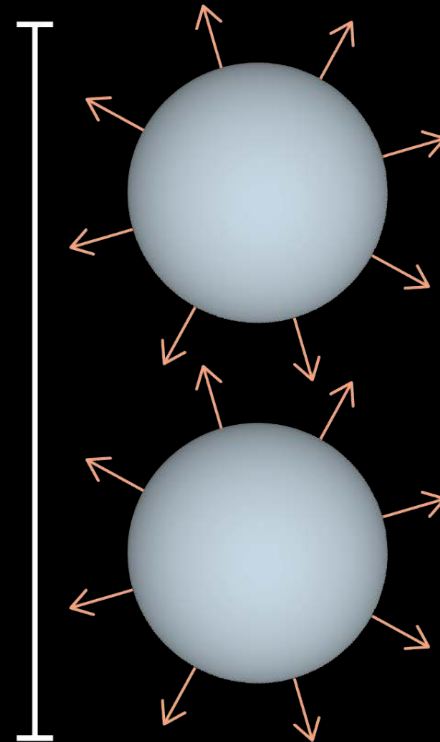
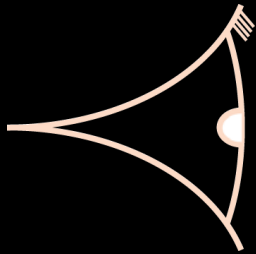


# Standard Raycasting

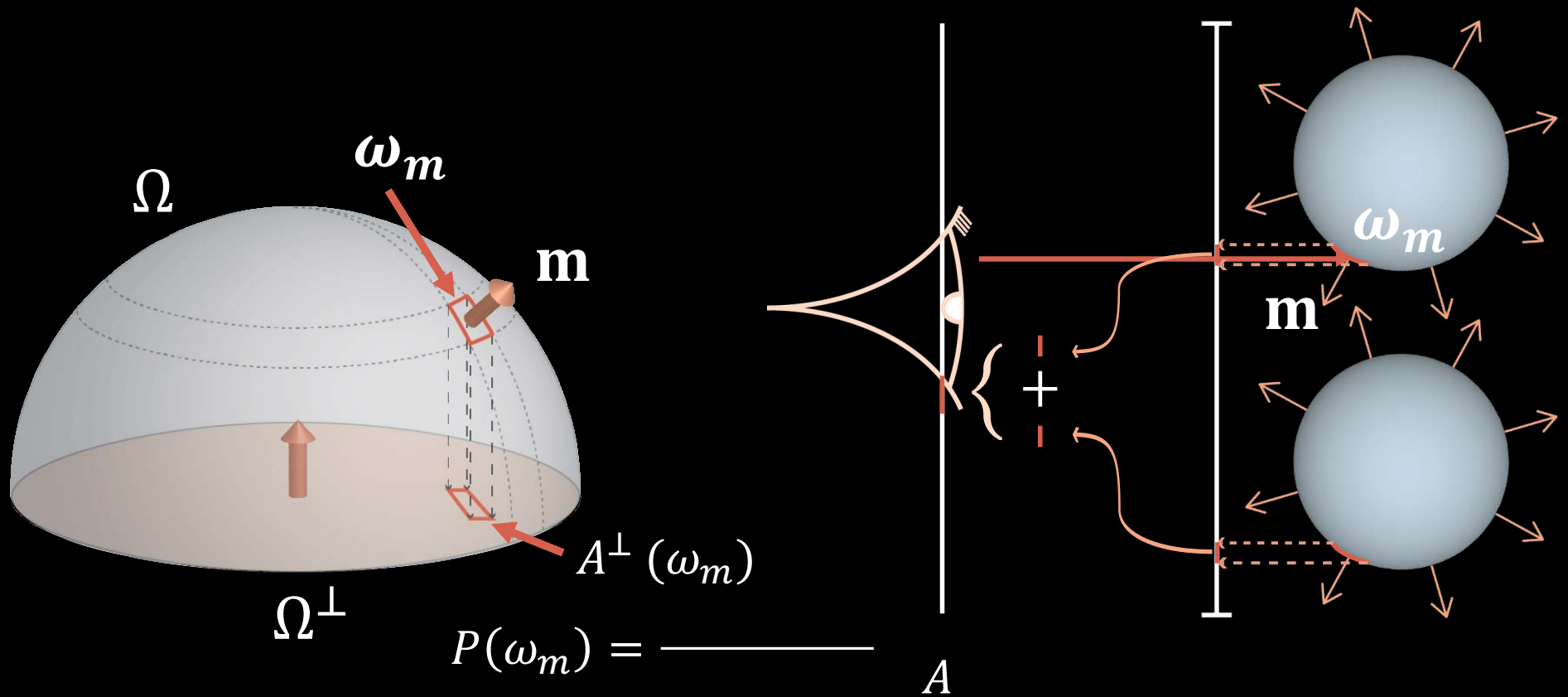
# Screen-Space Normal Distribution Functions (S-NDFs)



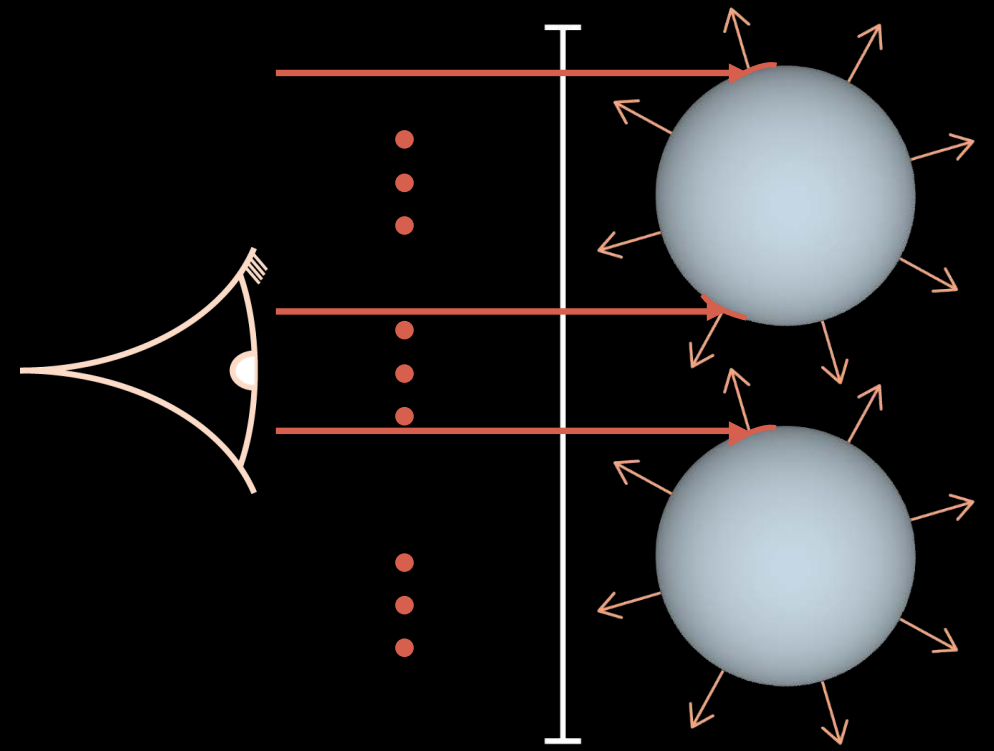
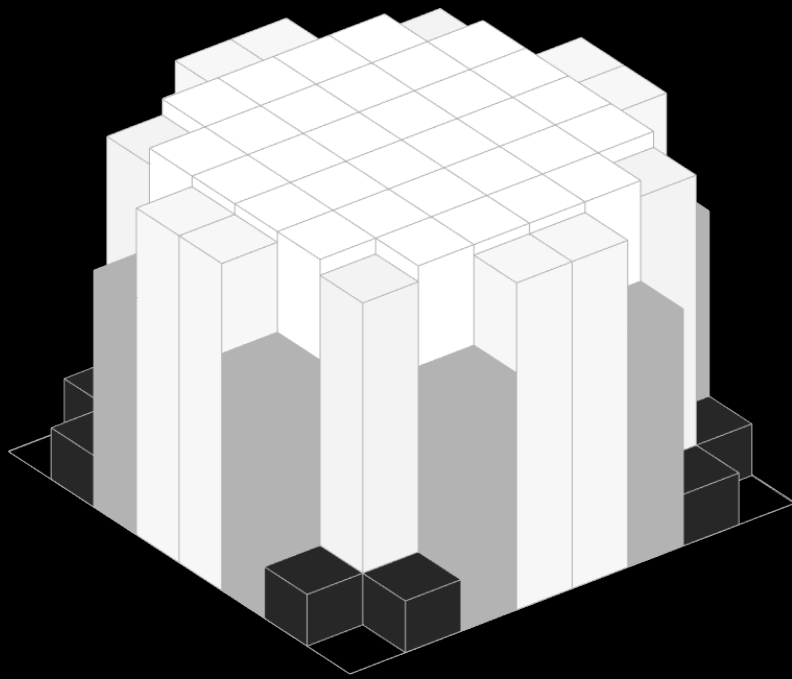
# Screen-Space Normal Distribution Functions (S-NDFs)



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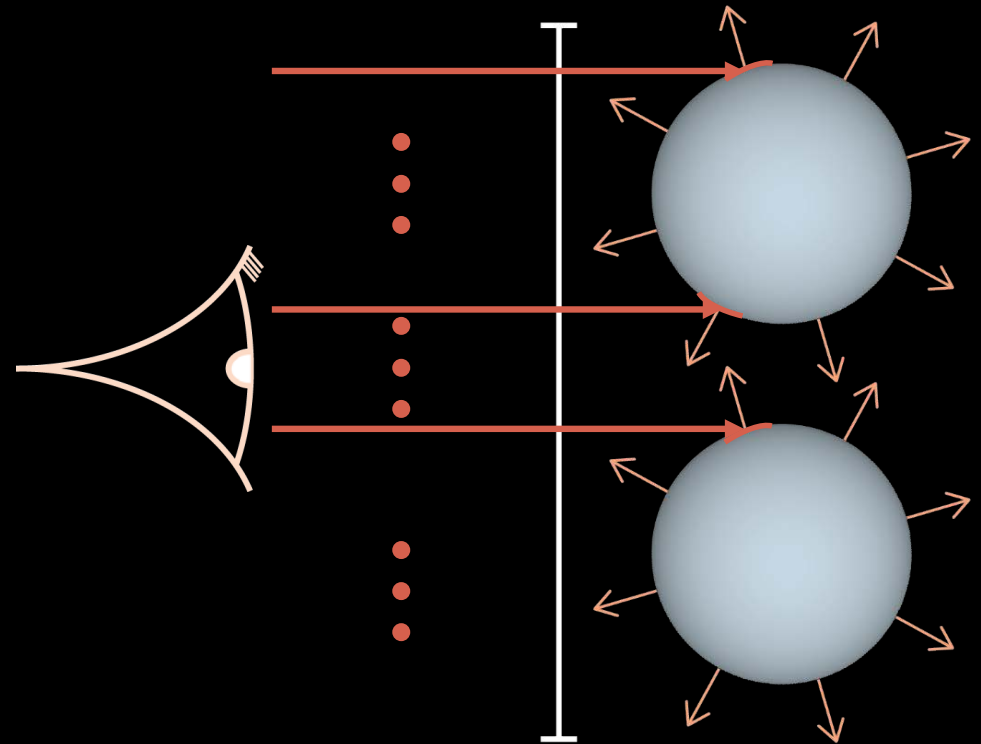
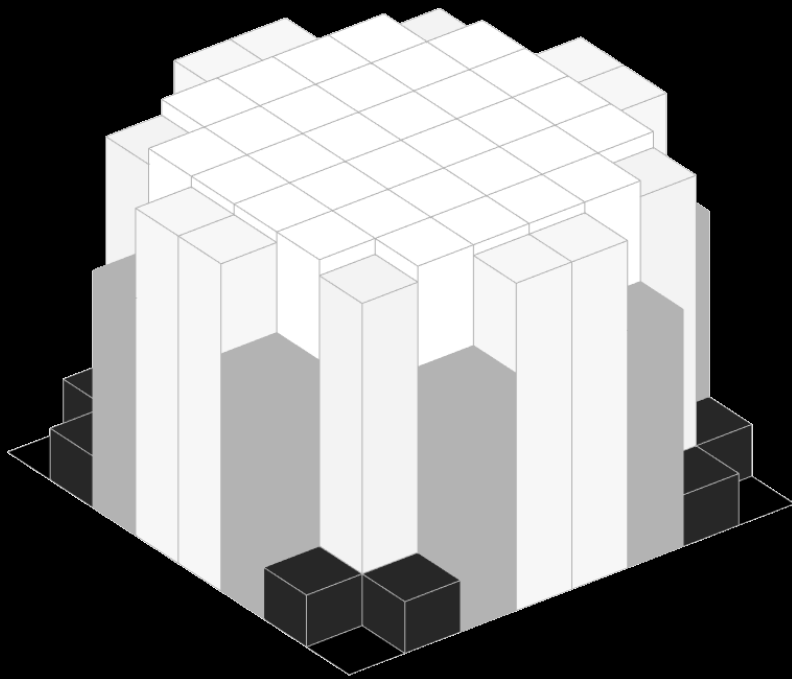


# Screen-Space Normal Distribution Functions (S-NDFs)





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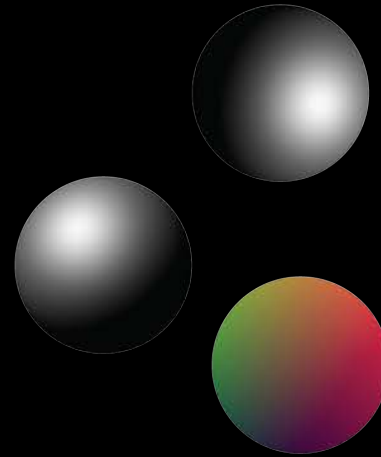


# Screen-Space Normal Distribution Functions (S-NDFs)



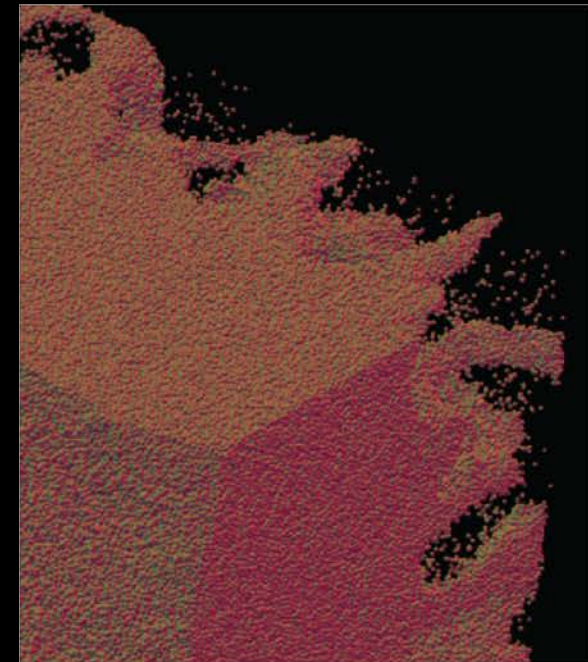
S-NDFs

\*



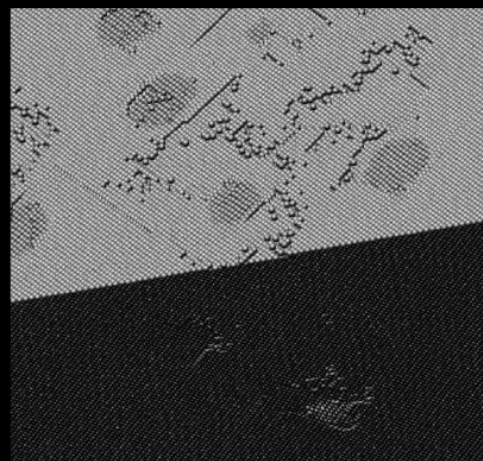
Transfer function

⇒



Rendered output

# Scale Consistency



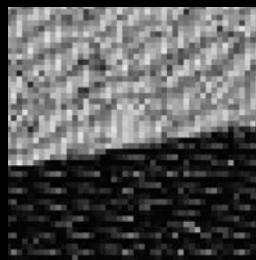
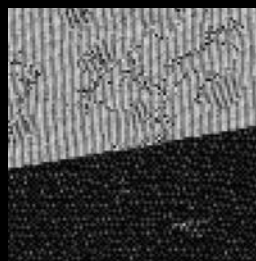
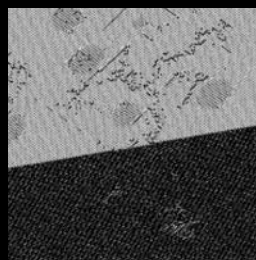
Lod 0

4x

8x

16x

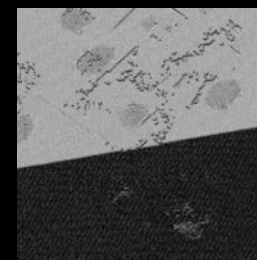
Raycasting  
(1 ray)



Raycasting  
( $4^{lod}$  rays)

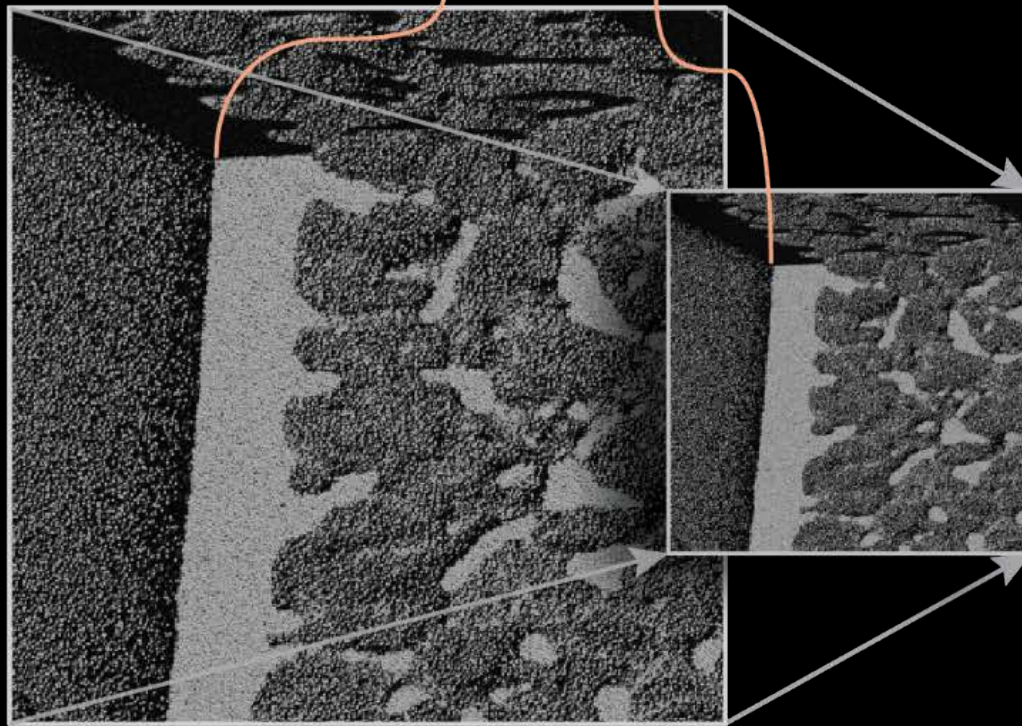


Our  
Approach

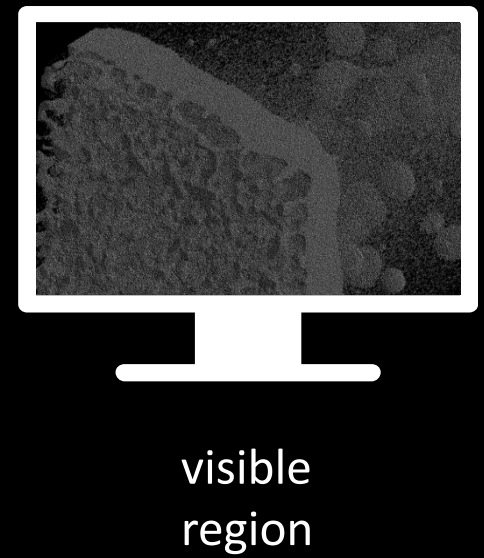
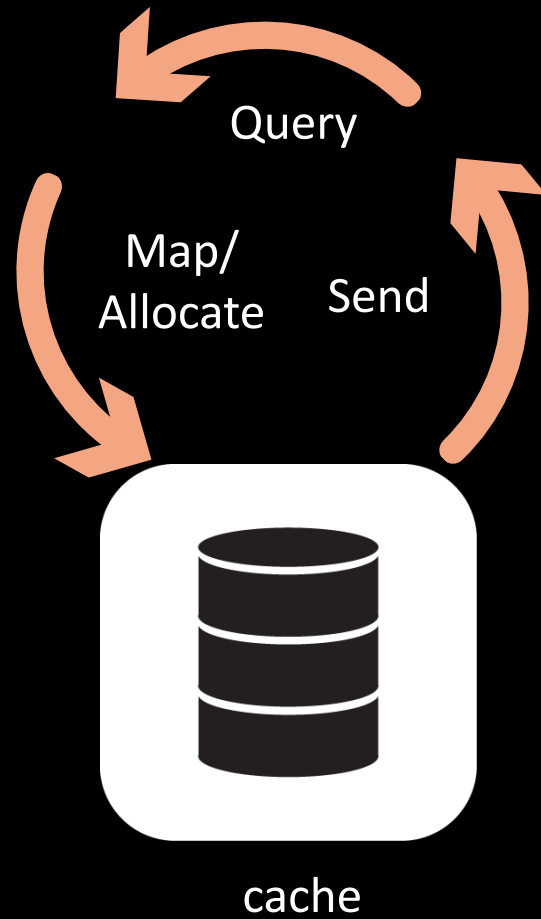
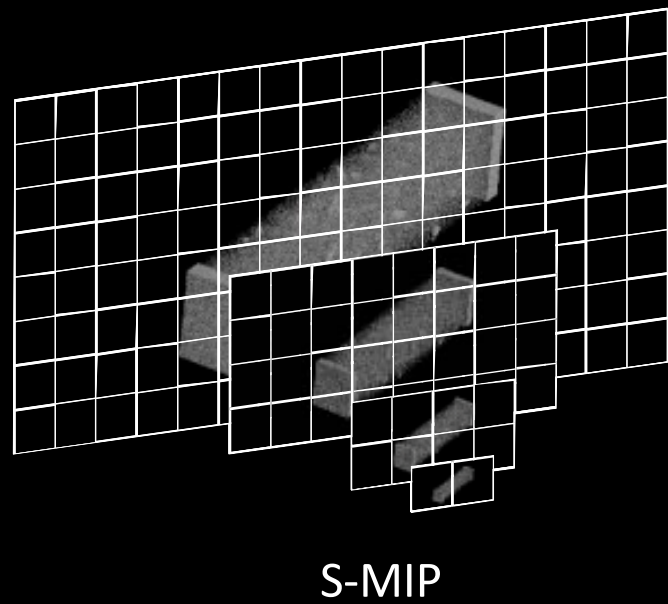


# Linearly Filtering S-NDFs

$$\frac{1}{4} \sum \begin{matrix} \text{[Top-Left Patch]} \\ \text{[Top-Right Patch]} \\ \text{[Bottom-Left Patch]} \\ \text{[Bottom-Right Patch]} \end{matrix} = \text{[Filtered Patch]}$$



# Caching S-NDFs

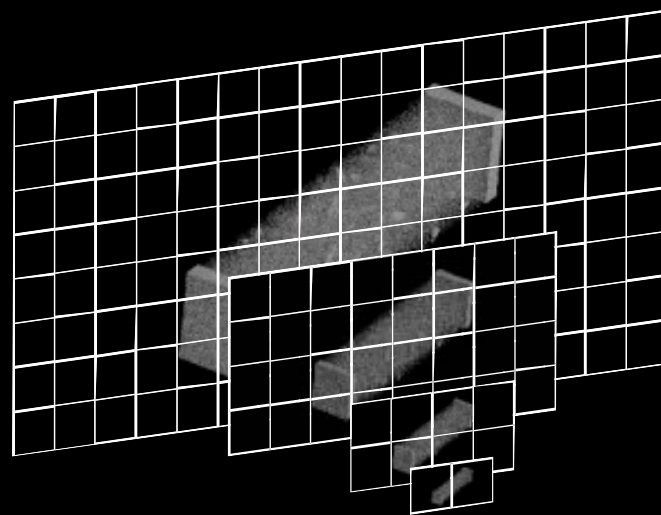


# Supported Operations



S-NDFs

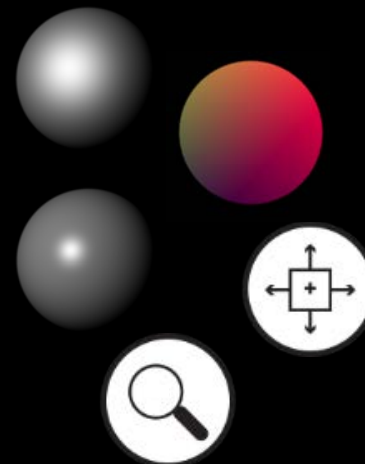
+



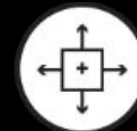
S-MIP



Relighting

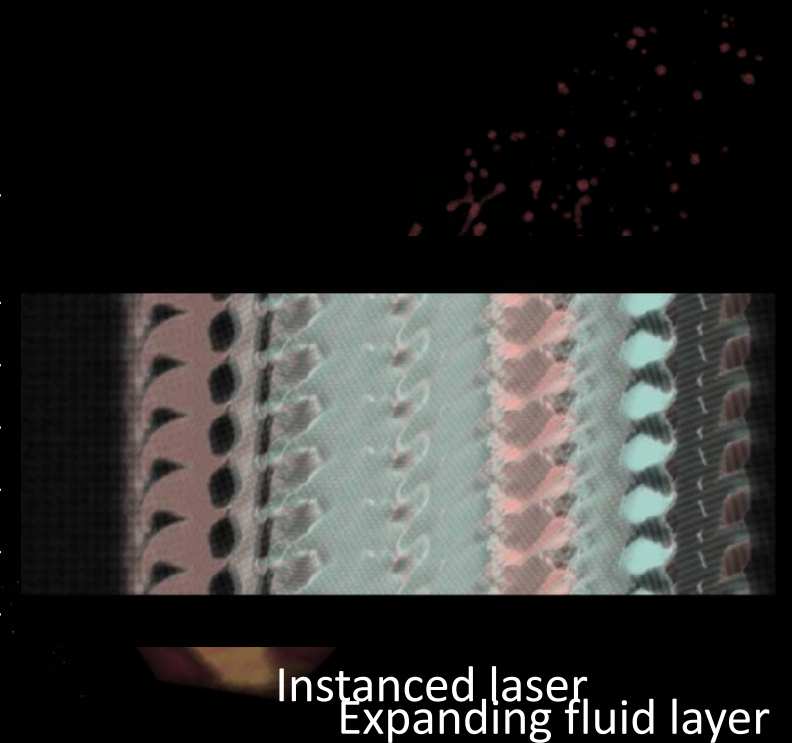


Navigational

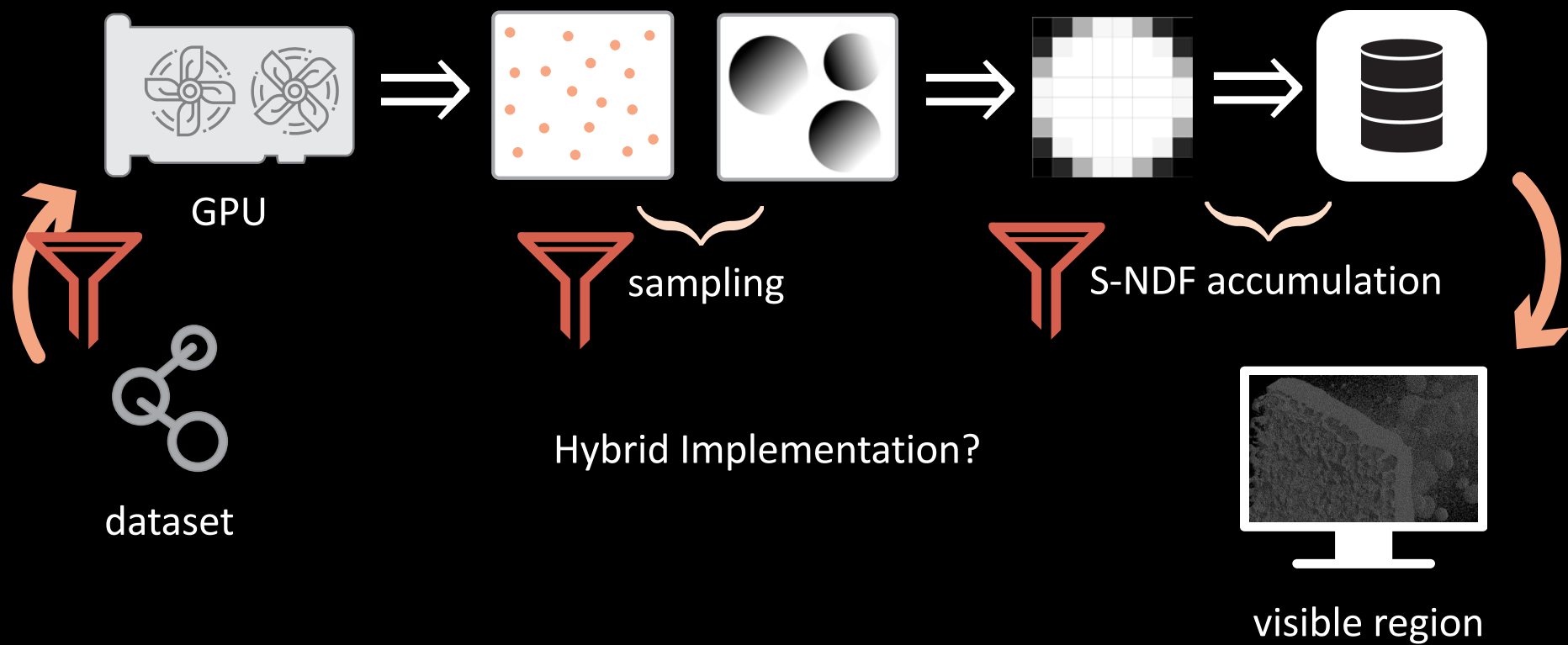


## Performance Measures (GPU)

data set	particle count	re-light [ms]	
		ray casting + S-MIP	S-NDF + S-MIP
Laser ablation crown	518,000	1129.74	26.53
Copper/silver mixture	14,500,00	1309.35	19.37
Expanding fluid layer	30,000,000	1523.61	22.19
Laser ablation	48,000,000	1253.84	22.17
Instanced laser (5×)	5× 12,500,000	1524.25	18.95
Large laser ablation	199,940.704	2203.66	16.87



# Implementation Details





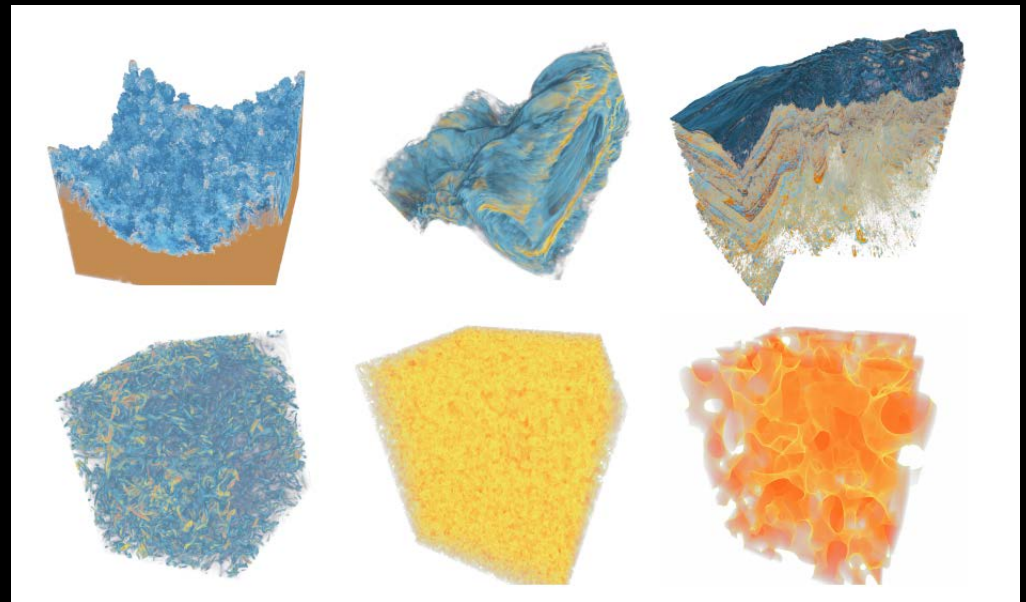
# OSPRay

Rendering API

Platform Independent

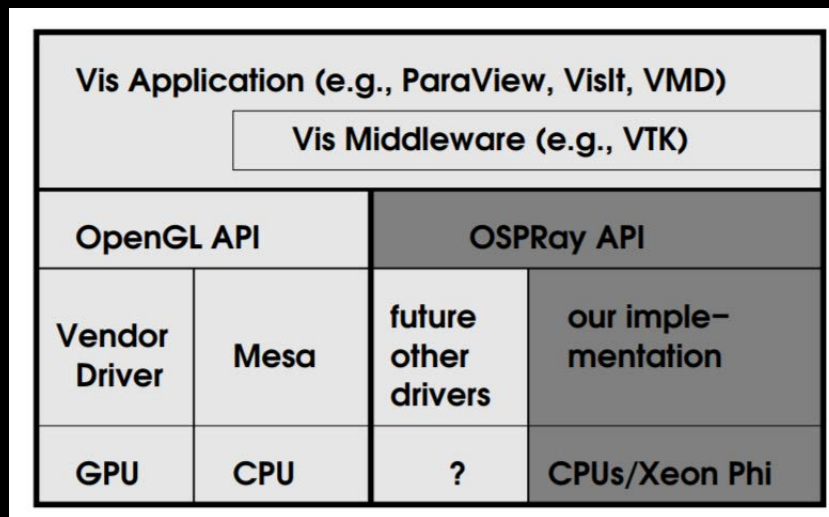
Visualization-oriented

CPU implementation

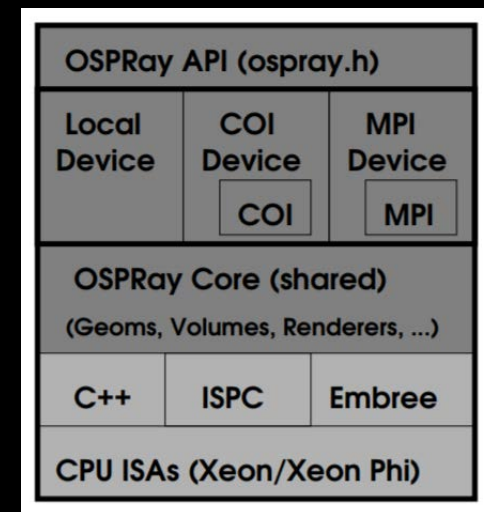


OSPRay – A CPU Ray Tracing Framework for Scientific Visualization.  
Wald, I. et al., IEEE Scientific Visualization 2016

# OSPRay ... Architecture



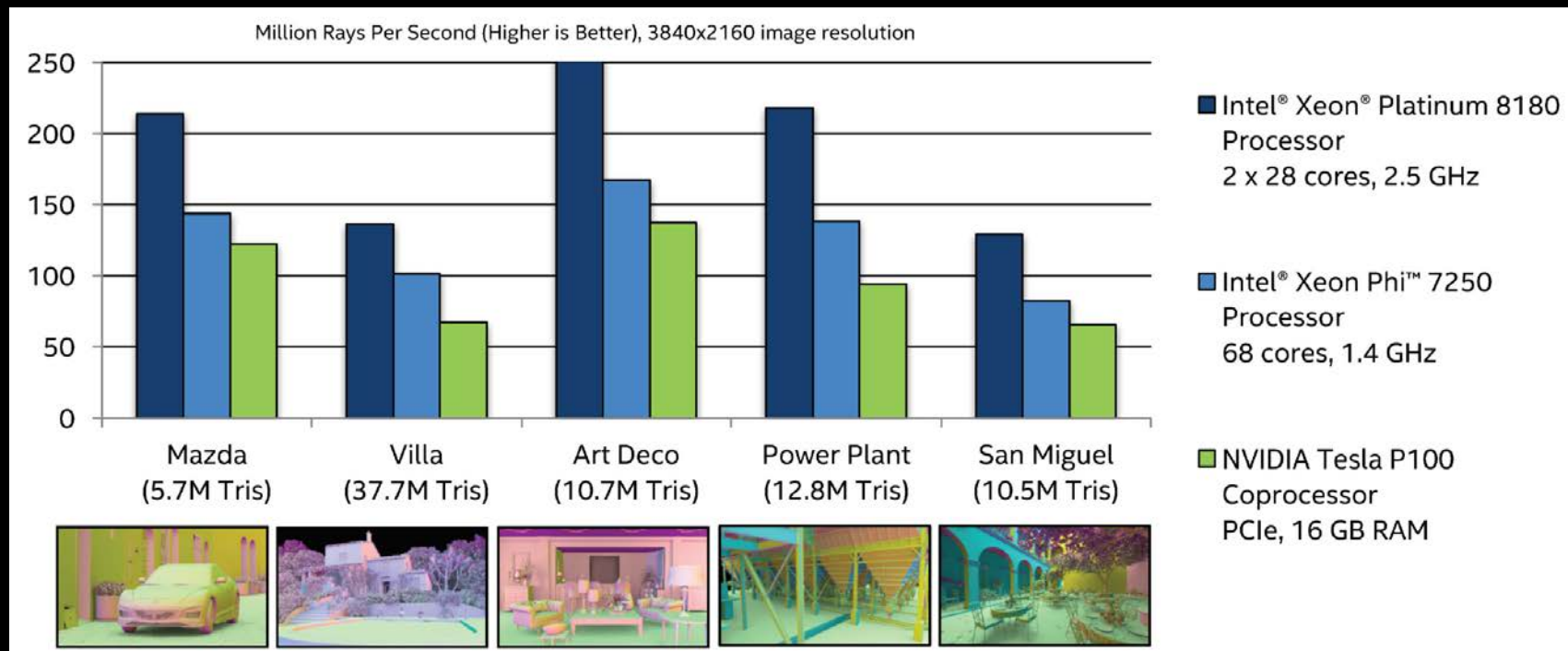
Rendering API



Device Abstraction

# OSPRay ... Performance

Diffuse Path Tracing Performance of Embree vs. NVIDIA OptiX Prime.

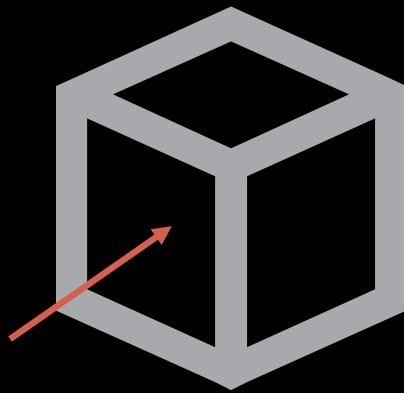


Embree: A Kernel Framework for Efficient CPU Ray Tracing.  
Wald, I. et al., ACM SIGGRAPH 2014

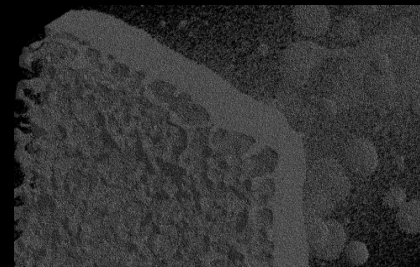
# OSPRay ... Integration



RTCBoundsFunc

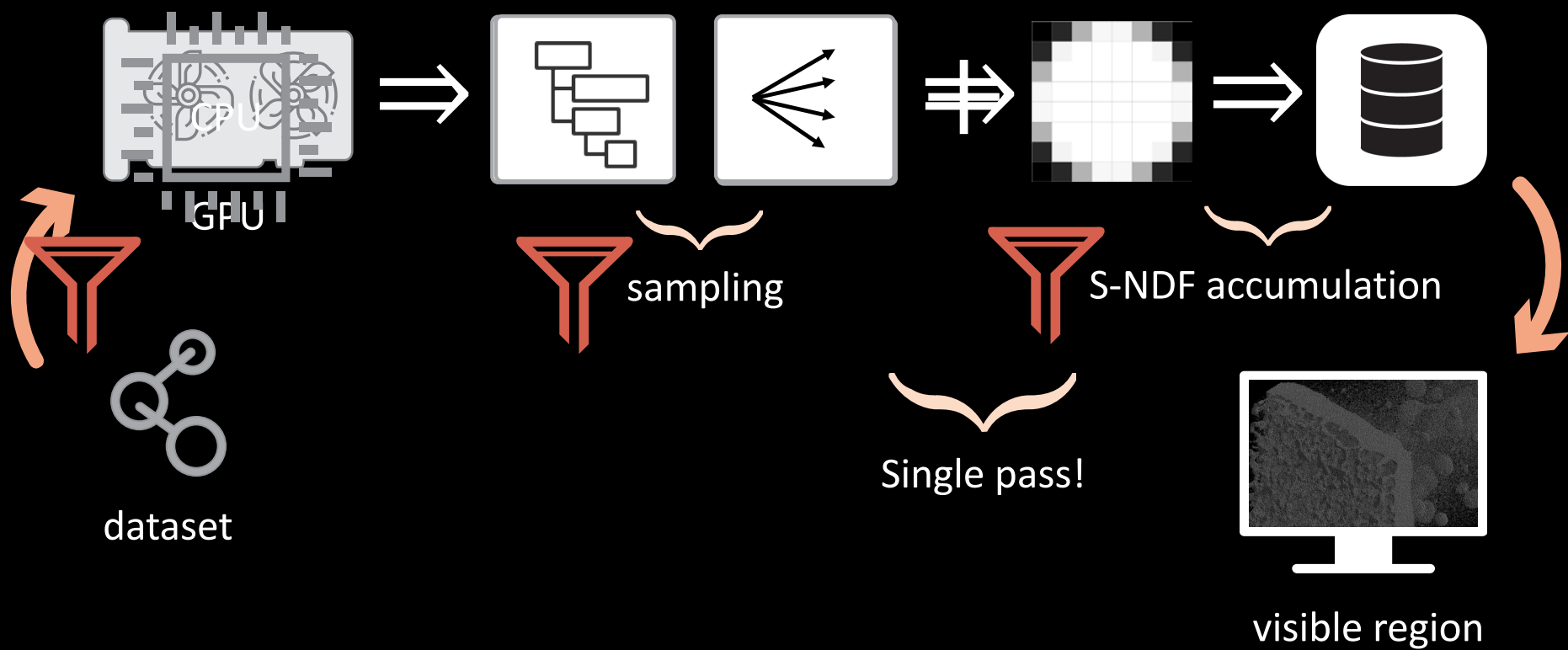


RTCIntersectFunc



RTCOccludedFunc

# OSPRay + S-NDFs + S-MIP?



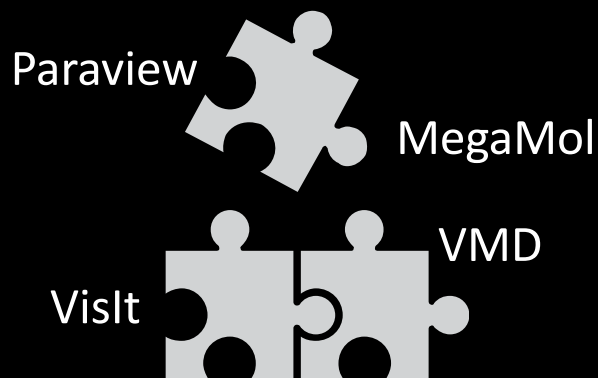
# OSPRay + S-NDFs + S-MIP?



Large data  
Large cache  
Finer S-NDFS  
4D S-NDFS



Fast traversal  
Multiple samples  
Guided sampling



Thank you

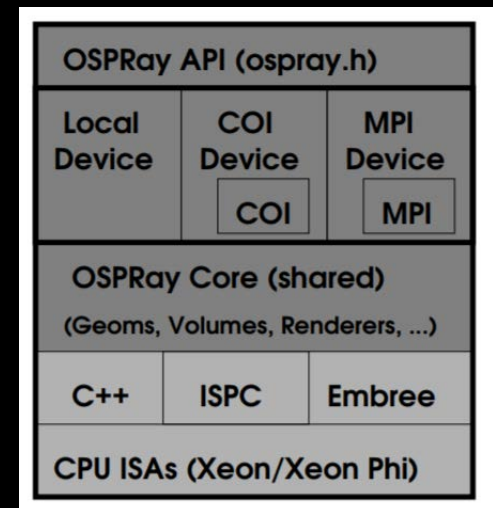
<http://www.vccvisualization.org>

## Application Scenarios



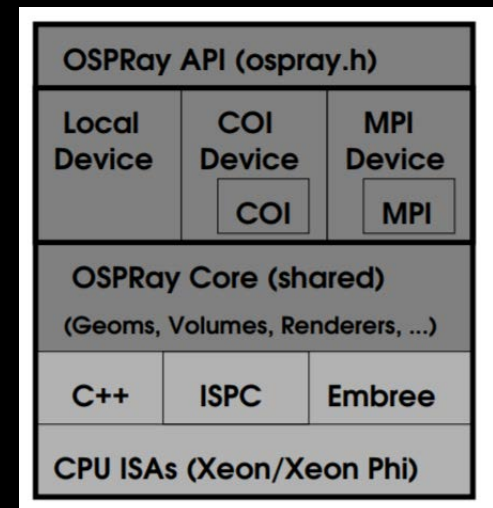
# Implementation ... Device Abstraction

- Ideal implementation differs according to target:
  - PCI-card based on Xeon Phi coprocessor
  - MPI-parallelism
- OSPRay supports device abstraction
  - API calls are seen as a stream of commands.
    - Each, internally, routed to one of multiple possible backend devices.



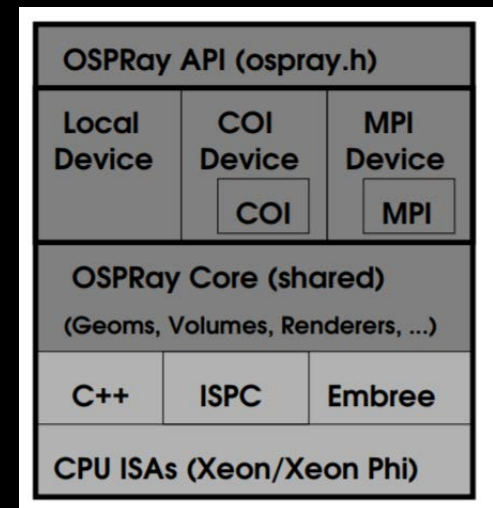
# Implementation ... Device Abstraction

- Local Device
  - Executes all rendering right in the same process as a the visualization application.
- COI Device
  - Offload to first-generation Xeon Phi Knights Corner coprocessor cards.
- MPIDevice
  - Support to MPI-parallel rendering
- All devices build on top of a shared rendering infrastructure that implements the actors.



# Software Infrastructure

- Build on top of
  - Intel SPMD Program Compiler (ISPC)
  - Embree ray tracing kernels
- Embree
  - Building and traversing acceleration structures.
  - Automatically selects acceleration structure and traversal kernels best suited for a given CPU.



# Software Infrastructure

- ISPC
  - All throughput sensitive operations that require vectorization (rendering, shading, primitive intersection)
  - Allows transparent targeting of multiple vector instruction set architectures (ISA).
    - Intel SSE4, AVX, AVX2, etc...

