GPAW performance optimisation and energy consumption on KNLs

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GPAW

• Density-functional theory (DFT) program for ab initio electronic structure calculations

• Code written mostly in Python
  o computational kernels in C
  o leverages external libraries (ScaLAPACK etc.)

• Parallelisation based on message-passing (MPI)

• Code freely available under GPL:
  https://gitlab.com/gpaw/gpaw

C60 fullerenes next to a Pb sheet
PRACE Accelerator Benchmarks

www.prace-ri.eu/ueabs/

• Unified European Applications Benchmark Suite (UEABS) developed by PRACE contains now benchmarks also aimed at accelerators

• For GPAW there are two benchmarks:
  o Small case: Carbon Nanotube (up to ~10 nodes)
  o Large case: Copper Filament (up to ~100 nodes)

• Both are ground state calculations in vacuum, but the Copper Filament benchmark is more computationally intensive (and able to scale up better)
Performance and Optimisation
Hardware

• ARCHER Knights Landing Testing and Development Platform by Cray
  o single 64-core KNL processor (Intel Xeon Phi 7210) running at 1.3GHz at each node
  o 96GB of standard memory per node
  o 16GB of high-bandwidth MCDRAM memory per KNL
  o 12 nodes in total, of which 8 in cache mode and 4 in flat mode

• Results compared to CSC's Sisu supercomputer (Cray XC40)
  o two 12-core Haswell CPUs (Intel Xeon E5-2690v3) running at 2.6GHz at each node
  o 64GB of standard DDR4 memory per node
Compiling Python and GPAW

• ARCHER's KNL system has Sandy Bridge login nodes, so GPAW and the underlying Python stack need to be built in two steps
  o Intel compiler (17.0.0) used for everything
  o Cray compiler wrapper (cc) takes care of correct compiler options (e.g. -xMIC-AVX512 on KNLs)

• Python+
  o target SNB (module load craype-sandybridge)

• GPAW
  o target KNL (module load craype-mic-knl)
  o memkind module is needed to get support for the high-bandwidth memory (module load cray-memkind)
Compiling Python and GPAW

• Intel TBB + huge pages
  o using huge pages together with the memory allocator from Intel TBB (tbbmalloc) allow for more optimised memory allocation on KNLs
  o for GPAW, performance increase is up to 5%
  o size of huge pages is not significant for GPAW (2M pages were used)
  o environment variable LD_PRELOAD was used to swap the standard memory allocator with the one from Intel TBB (no code modifications!)
Performance comparison, Haswell vs. KNL

<table>
<thead>
<tr>
<th>GPAW runtimes (in seconds) with n nodes</th>
<th>1</th>
<th>2</th>
<th>4</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>Carbon Nanotube</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Xeon E5-2690v3 x2</td>
<td>242.2</td>
<td>148.5</td>
<td>81.1</td>
<td>55.4</td>
</tr>
<tr>
<td>Xeon Phi 7210*</td>
<td>319.9</td>
<td>206.6</td>
<td>141.3</td>
<td>101.3</td>
</tr>
<tr>
<td>Copper Filament</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Xeon E5-2690v3 x2</td>
<td>405.0</td>
<td>191.5</td>
<td>86.9</td>
<td>60.5</td>
</tr>
<tr>
<td>Xeon Phi 7210*</td>
<td>323.4</td>
<td>172.3</td>
<td>127.0</td>
<td>80.0</td>
</tr>
</tbody>
</table>

*using tbbmalloc and 2M huge pages in CACHE / QUAD mode

- KNLs faster than CPUs for the *Copper Filament* benchmark when using one or two nodes
- Compared to CACHE mode, FLAT mode is over 50% slower (data not shown)
Code modifications

• Profiled with VTune Amplifier 2017 on KNLs and potential targets for optimisation were identified in the C kernels
  o triple nested loops with single step pointer incrementations to advance the position of input and/or output arrays

• Code changes:
  o use OpenMP SIMD pragmas
  o use explicit indexing instead of pointer incrementation OR do pointer incrementation in larger blocks at an upper loop level

• Allowed for better vectorisation of the loops by the compiler

• Obsolete, unnecessary code sections were also identified in the iterator and were removed

Merged to code base
Example code modifications to a kernel

```
for (int i1 = 0; i1 < s->n[1]; i1++)
{
    for (int i2 = 0; i2 < s->n[2]; i2++)
    {
        T x = 0.0;
        for (int c = 0; c < s->ncoefs; c++)
            x += aa[s->offsets[c]] * s->coefs[c];
        *bb++ = x;
        aa++;
    }
    aa += s->j[2];
}
```
Example code modifications to a kernel

① Explicit indexing in two inner-most loops

② Pointer incrementation at the outer loop level

③ OpenMP SIMD pragma to guide vectorisation of the two inner-most loops

```c
for (int i1 = 0; i1 < s->n[1]; i1++)
{
    // Explicit indexing

    // OpenMP SIMD pragma
    #pragma omp simd
    for (int i2 = 0; i2 < s->n[2]; i2++)
    {
        T x = 0.0;
        for (int c = 0; c < s->ncoefs; c++)
        {
            x += aa[s->offsets[c]] * s->coefs[c];
            *bb++ = x;
            aa++;
        }
        // Pointer incrementation
        x += aa[s->offsets[c] + i2] * s->coefs[c];
        bb[i2] = x;
    }
    // Pointer incrementation
    aa += s->j[2];
    bb += s->n[2];
    aa += s->j[2] + s->n[2];
}
```
Effects of OpenMP SIMD pragmas and explicit indexing

<table>
<thead>
<tr>
<th></th>
<th>GPAW runtimes (in seconds) and performance increase with n KNLs</th>
<th>up to 15-18% speed-up</th>
<th>load imbalance between the MPI tasks is now the main bottleneck</th>
</tr>
</thead>
<tbody>
<tr>
<td>Carbon Nanotube</td>
<td>reference: 319.9, 206.6, 141.3, 101.3</td>
<td>1.188, 1.165, 1.147, 1.110</td>
<td>Speed-up: 1.188, 1.165, 1.147, 1.110</td>
</tr>
<tr>
<td></td>
<td>optimised: 269.3, 177.3, 123.2, 91.3</td>
<td>1.152, 1.149, 1.094, 1.081</td>
<td>Speed-up: 1.152, 1.149, 1.094, 1.081</td>
</tr>
<tr>
<td>Copper Filament</td>
<td>reference: 323.4, 172.3, 127.0, 80.0</td>
<td>1.152, 1.149, 1.094, 1.081</td>
<td>Speed-up: 1.152, 1.149, 1.094, 1.081</td>
</tr>
<tr>
<td></td>
<td>optimised: 280.7, 150.0, 116.1, 74.0</td>
<td>1.152, 1.149, 1.094, 1.081</td>
<td>Speed-up: 1.152, 1.149, 1.094, 1.081</td>
</tr>
<tr>
<td>Reference on CPUs</td>
<td>Xeon E5-2690v3 x2</td>
<td>242.2, 148.5, 81.1, 55.4</td>
<td>Speed-up: 1.152, 1.149, 1.094, 1.081</td>
</tr>
<tr>
<td>Carbon Nanotube</td>
<td>Xeon E5-2690v3 x2</td>
<td>242.2, 148.5, 81.1, 55.4</td>
<td>Speed-up: 1.152, 1.149, 1.094, 1.081</td>
</tr>
<tr>
<td>Copper Filament</td>
<td>Xeon E5-2690v3 x2</td>
<td>405.0, 191.5, 86.9, 60.5</td>
<td>Speed-up: 1.152, 1.149, 1.094, 1.081</td>
</tr>
</tbody>
</table>
### GPAW on Skylake

<table>
<thead>
<tr>
<th></th>
<th>AVX-512</th>
<th>AVX-512*</th>
<th>AVX2</th>
<th>AVX2*</th>
<th>HSW</th>
<th>KNL*</th>
</tr>
</thead>
<tbody>
<tr>
<td>Carbon Nanotube</td>
<td>116.2</td>
<td>102.4</td>
<td>118.7</td>
<td>118.3</td>
<td>242.2</td>
<td>269.3</td>
</tr>
<tr>
<td>Copper Filament</td>
<td>156.8</td>
<td>153.7</td>
<td>150.3</td>
<td>150.1</td>
<td>405.0</td>
<td>280.7</td>
</tr>
</tbody>
</table>

*use code optimisations (OpenMP SIMDs & array indexing)

- Dual 26-core Skylake @ 2.1 GHz (Intel Xeon Platinum 8170) with 192 GB of DDR4 memory
  - HSW: dual 12-core Haswell @ 2.6 GHz (Intel Xeon E5-2690v3)
  - KNL: single 64-core Knights Landing @ 1.3 GHz (Intel Xeon Phi 7210)
- All results on Skylake and Knights Landing using tbbmalloc and 2M huge pages
Conclusions on performance
see full report at: github.com/cschpc/gpaw-on-KNL

• GPAW achieves similar performance on KNLs as on dual-CPU Haswell nodes, but with poorer scaling properties
  o Benchmarks with higher computational burden fare better on KNLs and also show better scaling properties

• Best performance achieved when using CACHE mode for MCDRAM and tbbmalloc with huge pages

• Some performance improvement (up to 18.8%) was achieved on KNLs by using OpenMP SIMDs and array indexing on three computational kernels
Hardware and software used for energy measurements

• PRACE Pre-Commercial Procurement (PCP) for energy efficient HPC solutions
  - Atos-Bull KNL pilot system (at CINES/GENCI)
  - E4 Power-8/Pascal pilot system (at CINECA)
  - Maxeler data-flow pilot system (at JUELICH)

• Atos-Bull KNL pilot system
  - 56 Atos-Bull Sequana X1210 blades + water-cooled power
  - 168 compute nodes with a single 68-core KNL (Intel Xeon Phi 7250) + HDEEM FPGA for energy monitoring

• Bull Energy Optimizer (BEO)
  - energy monitoring of the whole system (at 100Hz)
  - HDEEVIZ may be used for more detailed profiles (at 1kHz)
**Energy consumption & runtimes on PCP-KNL**

<table>
<thead>
<tr>
<th></th>
<th>1</th>
<th>2</th>
<th>4</th>
<th>8</th>
<th>16</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Carbon Nanotube</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>energy (kJ)</td>
<td>154</td>
<td>243</td>
<td>307</td>
<td>491</td>
<td>826</td>
<td>1800</td>
</tr>
<tr>
<td>runtime (s)</td>
<td>527.3</td>
<td>307.2</td>
<td>187.3</td>
<td>140.8</td>
<td>114.8</td>
<td>118.3</td>
</tr>
<tr>
<td><strong>Copper Filament</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>energy (kJ)</td>
<td>159</td>
<td>205</td>
<td>255</td>
<td>352</td>
<td>615</td>
<td>1200</td>
</tr>
<tr>
<td>runtime (s)</td>
<td>456.5</td>
<td>214.8</td>
<td>128.7</td>
<td>72.0</td>
<td>49.5</td>
<td>36.0</td>
</tr>
</tbody>
</table>

FLAT / QUAD mode

- Energy consumption seems to scale linearly with the number of KNLs used
- Absolute scaling limit reached for the *Carbon Nanotube* benchmark (< 32 KNLs)
Conclusions on energy consumption

• Energy consumption seems to grow linearly with the number of KNLs in use
  o maximum energy efficiency for runs with only a single KNL

• Minimum energy to solutions for the PRACE accelerator benchmarks on the PCP-KNL in FLAT/QUAD mode:
  o Carbon Nanotube:  (154 +/- 3) kJ
  o Copper Filament:  (159 +/- 3) kJ

• Slightly lower energy to solution results expected for KNLs running in CACHE mode instead of the FLAT mode (simply due to faster run times)
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