SCALING COLLECTIVES ON LARGE CLUSTERS USING INTEL(R) ARCHITECTURE PROCESSORS AND FABRIC

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System: One of World largest Intel® Xeon Phi™ + Intel® Omni-Path Architecture (Intel® OPA) system => OakForest-PACS

8208 node of Intel Xeon Phi (KNL) 7250 (68c, 1.4GHz) with full bi-section BW fat tree and 26PB Lustre by single rail Intel OPA interconnect. CentOS 7.2 on compute node.

25PFLOPS peak and #6 in Top 500 at launch

*Detail configuration in backup slides*
Initial results: Run-to-run variability

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Intel MPI Benchmark (IMB) Barrier and 16 Byte Allreduce. 1 rank per node.

4 groups of 2048 node

Almost same latency in each group would be expected but...

Group to group variance would be less significant than inside group

Wide variances due to OS noise? (hypothesize)
Initial results: performance

IMB barrier and 16B allreduce results.
1 process per node.

Ideal \( \log_2(N) \), \( N \): rank

OS noise increases non-linearly

No good explanation for worse barrier scaling than allreduce at high count
Initial investigation

// Recording time for each iteration on each rank

MPI_Barrier(MPI_COMM_WORLD);
tscs[0] = _rdtsc();
for (int i = 0; i < ntimes; ++i) {
    MPI_Barrier(MPI_COMM_WORLD);
    tscs[i+1] = _rdtsc();
}
report (rank, nranks, ntimes, tscs, benchmark, 0);

• Extreme excursions from mean are due to OS noise
• Kernel trace verified correlation with this
Cause of variance

ps, top, Vtune, kernel ftrace analysis used to find 3 major sources of variance

- **Frequency transition (Turbo):** 1.4GHz $\rightarrow$ 1.5GHz $\rightarrow$ 1.6GHz
  Transition stalls many microseconds.

- **Periodic MWAIT wake-up:**
  Linux system default is using idle=mwait. MONITOR and MWAIT instructions on idle hardware threads.
  KNL forces a periodic wake-up of hardware threads in an MWAIT state 10 times per second and additionally cause frequency transitions on the entire processor.

- **OS work:**
  Daemons, hardware interrupts, middleware (system monitoring, scheduling). idle thread on the same core or tile is awakened to perform OS work, the application thread will be delayed and additionally cause frequency transitions.

Simulated barrier results by recursive doubling. Theoretical: $\log_2(\text{# of node}) \times \text{Latency}$. 20K cycle injected with probability $p$ at each step. $L=3.5\mu\text{sec}, 20\text{K cycle}=14\mu\text{sec}$.
Remedies

idel=halt: Stopping MONIOTR/MWAIT and single-tile turbo (No 1.6GHz)

Tickless mode (nohz_full=2-67,70-135,138-203,206-271): Decreasing OS timer interrupt from 1KHz to 1Hz except tile-0. And excluding tile-0 from application.

Binding Lustre daemon and system process to tile-0

Using acpi-cpufreq driver rather than intel_pstate

Tuning spinning: PSM2_YIELD_SPIN_COUNT=10000 and I_MPI_COLL_SHM_PROGRESS_SPIN_COUNT=100000

* These remedies have cons side effects (effect depends on situation and application).
Run to run variability improvement on 4096 node

Applying remedies, run to run variability was largely improved
+-4% from median now
Performance Results

HT ON result with iMPI 2017U3 improved hugely (7.1x and 3.3x) vs. baseline.

HT OFF with iMPI 2017U3 better than HT ON.

8K node allreduce has still some noise even with HT OFF.

By MPI library tuning (reduced # of inst), HT ON with iMPI2019TP matched HT OFF (iMPI2017U3) result.

Future work: HT OFF with iMPI2019 and multi process per node

<table>
<thead>
<tr>
<th>4K node collective</th>
<th>Target [usec]</th>
<th>Baseline [usec]</th>
<th>Optimized [usec]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Barrier</td>
<td>105</td>
<td>671</td>
<td>94</td>
</tr>
<tr>
<td>16B Allreduce</td>
<td>160</td>
<td>485</td>
<td>145</td>
</tr>
</tbody>
</table>
System and MPI library optimizations on large scale KNL+OPA cluster achieved 7.1x and 3.3x improvement for IMB barrier and 16B allreduce on 4K node.

Call to action:

- Read carefully “latest” Intel® Omni-Path Fabric Performance Tuning User Guide (now Rev. 10.0, Oct. 2017)
- Provide suggestions to masashi.horikoshi@intel.com and lawrence.f.meadows@intel.com
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## Specification of Oakforest-PACS system

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total peak performance</td>
<td>25 PFLOPS</td>
</tr>
<tr>
<td>Total number of compute nodes</td>
<td>8,208</td>
</tr>
</tbody>
</table>

**Compute node**

<table>
<thead>
<tr>
<th>Product</th>
<th>Fujitsu PRIMERGY CX600 M1 (2U) + CX1640 M1 x 8node</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processor</td>
<td>Intel® Xeon Phi™ 7250 (Code name: Knights Landing), 68 cores, 1.4 GHz</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Memory</th>
<th>High BW</th>
<th>Low BW</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>16 GB, 490 GB/sec (MCDRAM, effective rate)</td>
<td>96 GB, 115.2 GB/sec (peak rate)</td>
</tr>
</tbody>
</table>

**Interconnect**

<table>
<thead>
<tr>
<th>Product</th>
<th>Intel® Omni-Path Architecture</th>
</tr>
</thead>
<tbody>
<tr>
<td>Link speed</td>
<td>100 Gbps</td>
</tr>
<tr>
<td>Topology</td>
<td>Fat-tree with (completely) full-bisection bandwidth</td>
</tr>
</tbody>
</table>

Slide courtesy of Prof. Hanawa and Prof. Boku
Full bisection bandwidth Fat-tree by Intel® Omni-Path Architecture

12 of 768 port Director Switch (Source by Intel)

362 of 48 port Edge Switch

Firstly, to reduce switches & cables, we considered:
- All the nodes into subgroups are connected with FBB Fat-tree
- Subgroups are connected with each other with >20% of FBB
  But, HW quantity is not so different from globally FBB, and globally FBB is preferred for flexible job management.

Compute Nodes | 8208
Login Nodes | 20
Parallel FS | 64
IME | 300
Mgmt, etc. | 8
Total | 8600

Slide courtesy of Prof. Hanawa and Prof. Boku
### Specification of Oakforest-PACS system (Cont’d)

<table>
<thead>
<tr>
<th>Parallel File System</th>
<th>Type</th>
<th>Lustre File System</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Capacity</td>
<td>26.2 PB</td>
<td></td>
</tr>
<tr>
<td>Product</td>
<td>DataDirect Networks ES14K</td>
<td></td>
</tr>
<tr>
<td>Aggregate BW</td>
<td>500 GB/sec (50 GB/sec x 10 OSS)</td>
<td></td>
</tr>
<tr>
<td>Metadata</td>
<td>MDS x 12, MDT x 3, 3 DNE (Distributed Namespace)</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>File Cache System</th>
<th>Type</th>
<th>Burst Buffer, Infinite Memory Engine (by DDN)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total capacity</td>
<td>940 TB (NVMe SSD, including parity data by erasure coding)</td>
<td></td>
</tr>
<tr>
<td>Product</td>
<td>DataDirect Networks IME14K</td>
<td></td>
</tr>
<tr>
<td>Aggregate BW</td>
<td>1,560 GB/sec (with 25 x2 IME servers)</td>
<td></td>
</tr>
<tr>
<td>Power consumption</td>
<td>4.2 MW (including cooling)</td>
<td></td>
</tr>
<tr>
<td># of racks</td>
<td>102</td>
<td></td>
</tr>
</tbody>
</table>

Slide courtesy of Prof. Hanawa and Prof. Boku
Acknowledgements

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