



# EARTHQUAKE SIMULATIONS ON THE INTEL XEON PHI PROCESSOR

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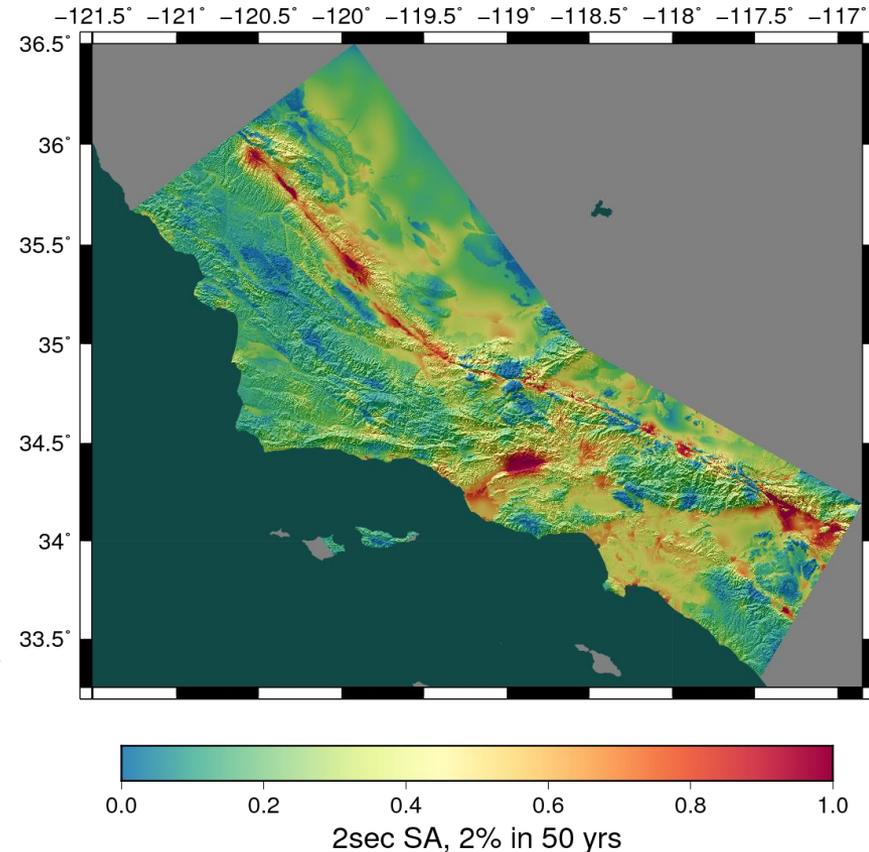
Notice revision #20110804

# What is AWP-ODC-OS?

AWP-ODC-OS (Anelastic Wave Propagation, Olsen, Day, Cui):  
Simulates seismic wave propagation after a fault rupture

Used extensively by the  
Southern California  
Earthquake Center community  
(SCEC)

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[Combined Hazard map](#) of CyberShake Study 15.4 (LA, CVM-S4.26) and CyberShake Study 17.4 (Central California, CCA-06). AWP-ODC simulations are used to generate hazard maps. Colors show 2 seconds period spectral acceleration (SA) for 2% exceedance probability in 50 years.

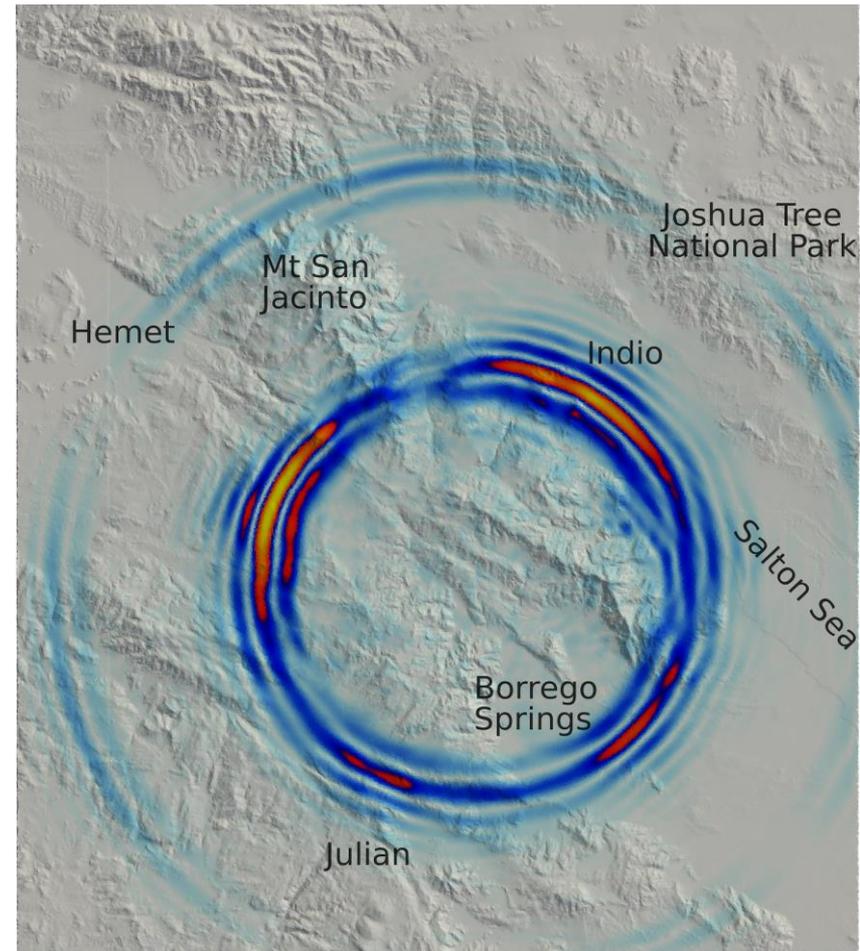
# What is EDGE?

Extreme-scale Discontinuous  
Galerkin Environment (EDGE):  
Seismic wave propagation  
through DG-FEM

Focus: Problem settings with high  
geometric complexity, e.g.,  
mountain topography

“License”: BSD 3-Clause  
(software), CC0 for supporting  
files (e.g., user guide)

<http://dial3343.org>



Example of hypothetical seismic wave propagation with mountain topography using EDGE. Shown is the surface of the computational domain covering the San Jacinto fault zone between Anza and Borrego Springs in California. Colors denote the amplitude of the particle velocity, where warmer colors correspond to higher amplitudes.

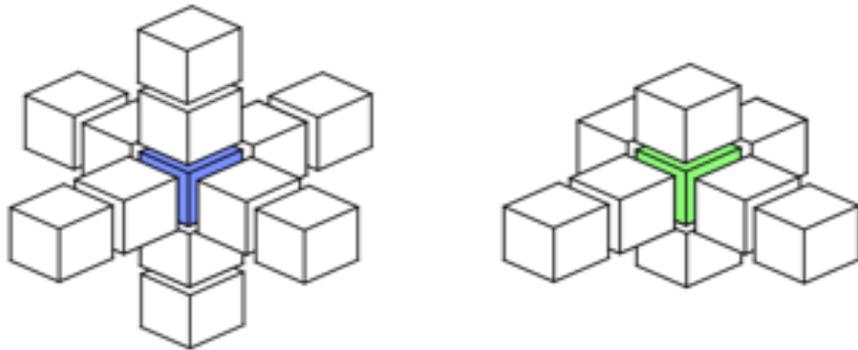
# Two Representative Codes

**AWP-ODC-OS**

Finite difference scheme: 4th order in space, 2nd order in time

Staggered-grid, velocity/stress formulation of elastodynamic eqns with frequency dependent attenuation

Memory bandwidth bound

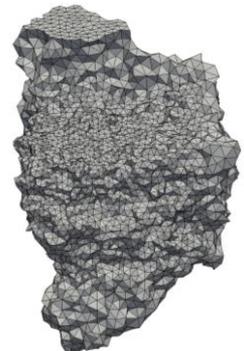
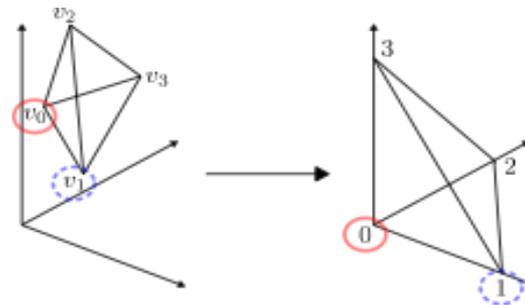


**EDGE**

Discontinuous Galerkin Finite Element Method (DG-FEM)

Unstructured tetrahedral meshes  
Small matrix kernels in inner loops

Compute bound for higher orders



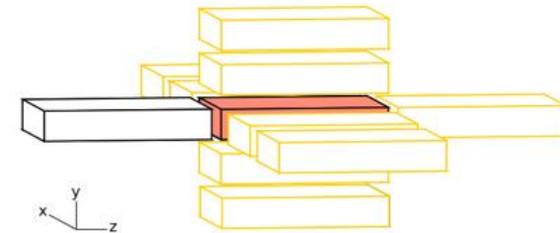
# Boosting Single-Node Performance: Vector Folding

- Vector folding data layout
  - Stores elements in small SIMD-sized multi-dimensional blocks
  - Reduces memory bandwidth demands by increasing reuse
- YASK (Yet Another Stencil Kernel)
  - Open-source (MIT License) framework from Intel
  - Inputs scalar stencil code
  - Creates optimized kernels using vector folding and other optimizations



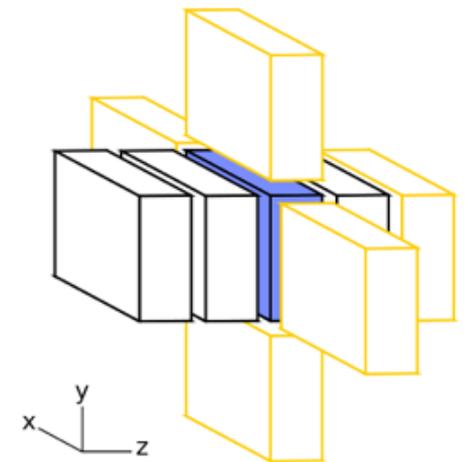
<https://github.com/01org/yask>

Traditional  
vectorization



Requires 9 cache loads per SIMD result

Two-  
dimensional  
Vector folding



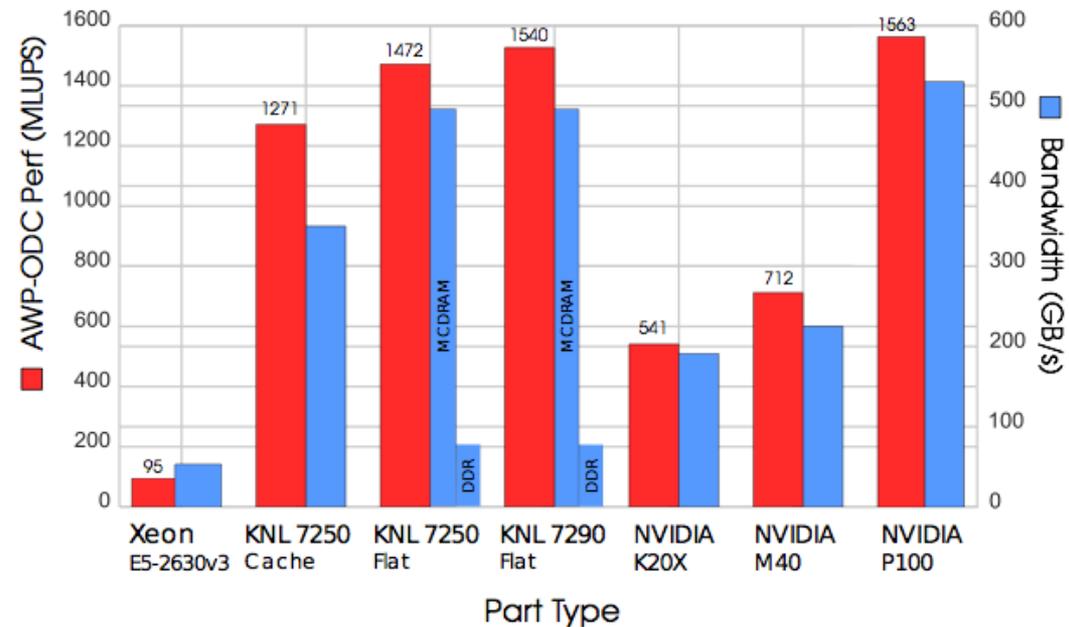
Requires only 5 cache loads

# Architecture Comparison

Xeon Phi KNL 7290:

2x speedup over  
NVIDIA K20X; 97% of  
NVIDIA Tesla P100  
performance

Memory bandwidth  
accurately predicts  
performance of  
architectures (as  
measured by STREAM  
and HPCG-SpMv)



Single node performance comparison of AWP-ODC-OS on a variety of architectures. Also displayed is the bandwidth of each architecture, as measured by a STREAM and HPCG-SpMv [ISC\_17\_2].

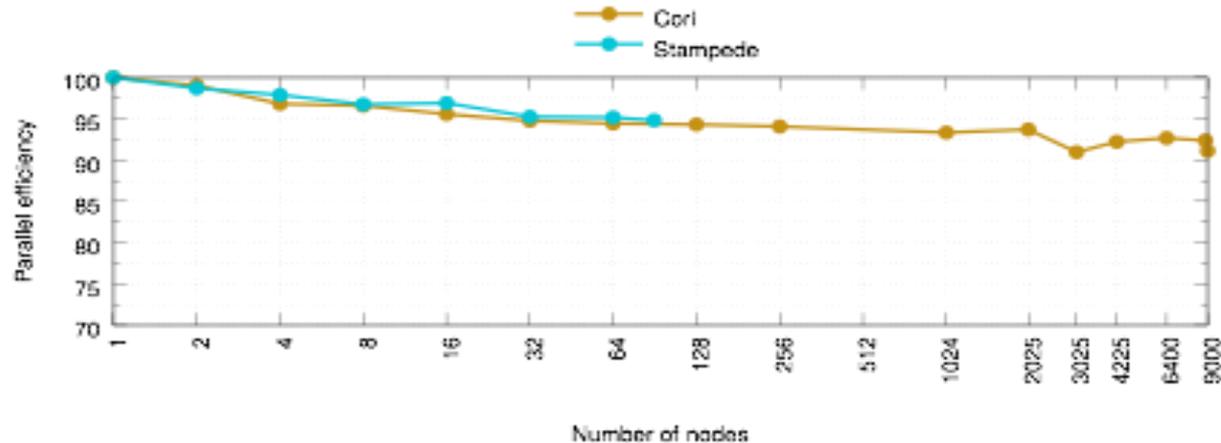
# Outperforming 20K GPUs

Weak scaling studies on NERSC  
Cori Phase II and TACC  
Stampede Extension

Parallel efficiency of over 91%  
from 1 to 9000 nodes (9000  
nodes = 612,000 cores)

Problem size of 512x512x512  
per node (14 GB per node)

Performance on 9000 nodes of  
Cori equivalent to  
performance of over 20,000  
K20X GPUs at 100% scaling



AWP-ODC-OS weak scaling on Cori Phase II and TACC Stampede. We attain 91% scaling from 1 to 9000 nodes. The problem size required 14GB on each node [ISC\_17\_2].

# Fused Simulations

Exploits inter-simulation parallelism:

- Full vector operations, even for sparse matrix operators
- Automatic memory alignment
- Read-only data shared among all runs
- Lower sensitivity to latency (memory & network)

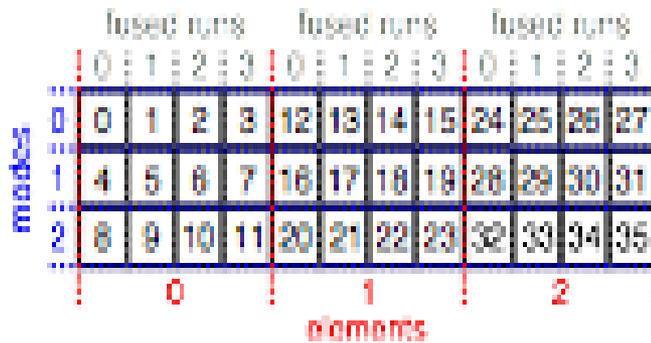
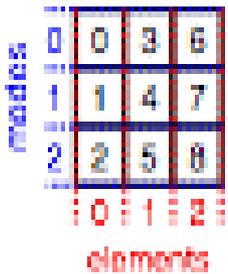


Illustration of the memory layout for fused simulations in EDGE. Shown is a third order configuration for line elements and the advection equation. Left: Single forward simulation, right: 4 fused simulations

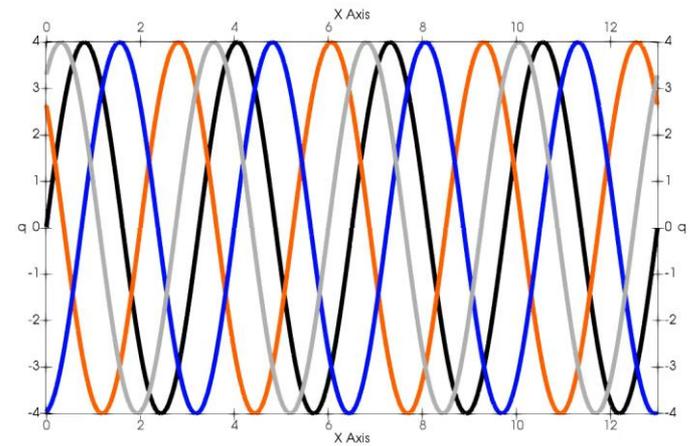
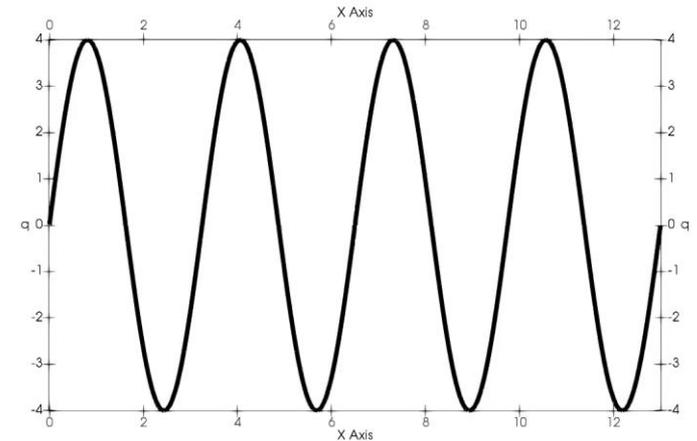


Illustration of fused simulations in EDGE for the advection equation using line elements. Top: Single forward simulation, bottom: 4 fused simulations.

# Fused Simulations: Performance

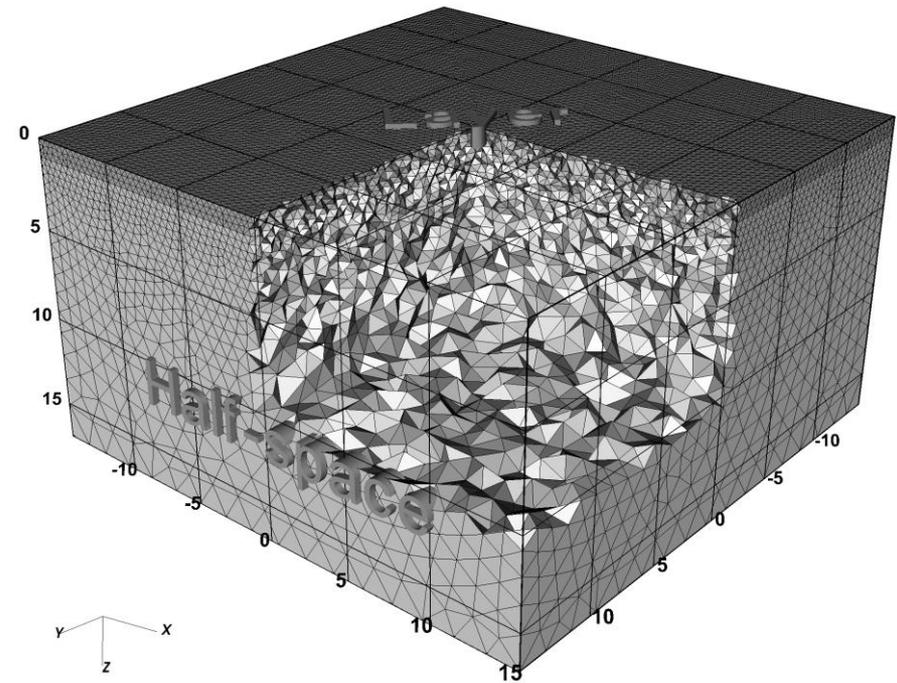
Orders: 2-6 (non-fused), 2-4 (fused)

Unstructured tetrahedral mesh: 350,264 elements

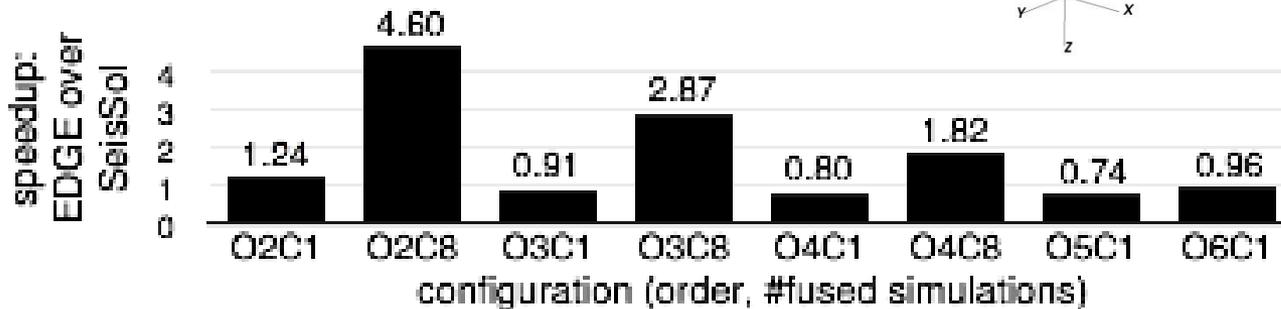
Single node of Cori-II (68 core Intel Xeon Phi x200, code-named Knights Landing)

EDGE vs. SeisSol (GTS, git-tag 201511)

Speedup: 2-5x



LOH.1 Benchmark: Example mesh and material regions [ISC16\_1]



Speedup of EDGE over SeisSol (GTS, git-tag 201511). Convergence rates O2 – O6: single non-fused forward simulations (O2C1-O6C1). Additionally, per-simulation speedups for orders O2–O4 when using EDGE’s full capabilities by fusing eight simulations (O2C8-O4C8). [ISC17\_1]

# Reaching 10+ PFLOPS

Regular cubic mesh, 5 Tets  
per Cube, 4th order (O4)  
and 6th order (O6)

Imitates convergence  
benchmark

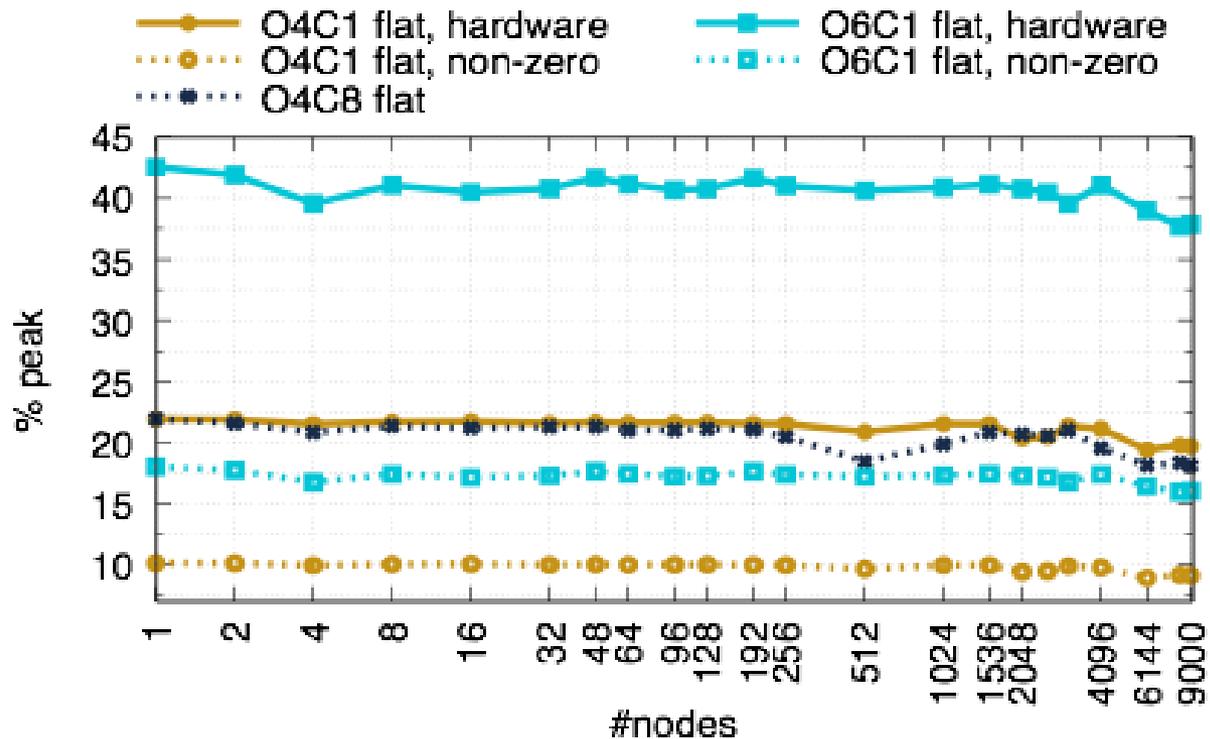
276K elements per node

1-9000 nodes of Cori-II (9000  
nodes = 612,000 cores)

O6C1 @ 9K nodes: 10.4  
PFLOPS (38% of peak)

O4C8: @ 9K nodes: 5.0  
PFLOPS (18% of peak)

O4C8 vs. O4C1 @ 9K nodes:  
2.0x speedup



Weak scaling study on Cori-II. Shown are hardware and non-zero peak efficiencies in flat mode. O denotes the order and C the number of fused simulations [ISC17\_1].

# Strong at the Limit: 50x and 100x

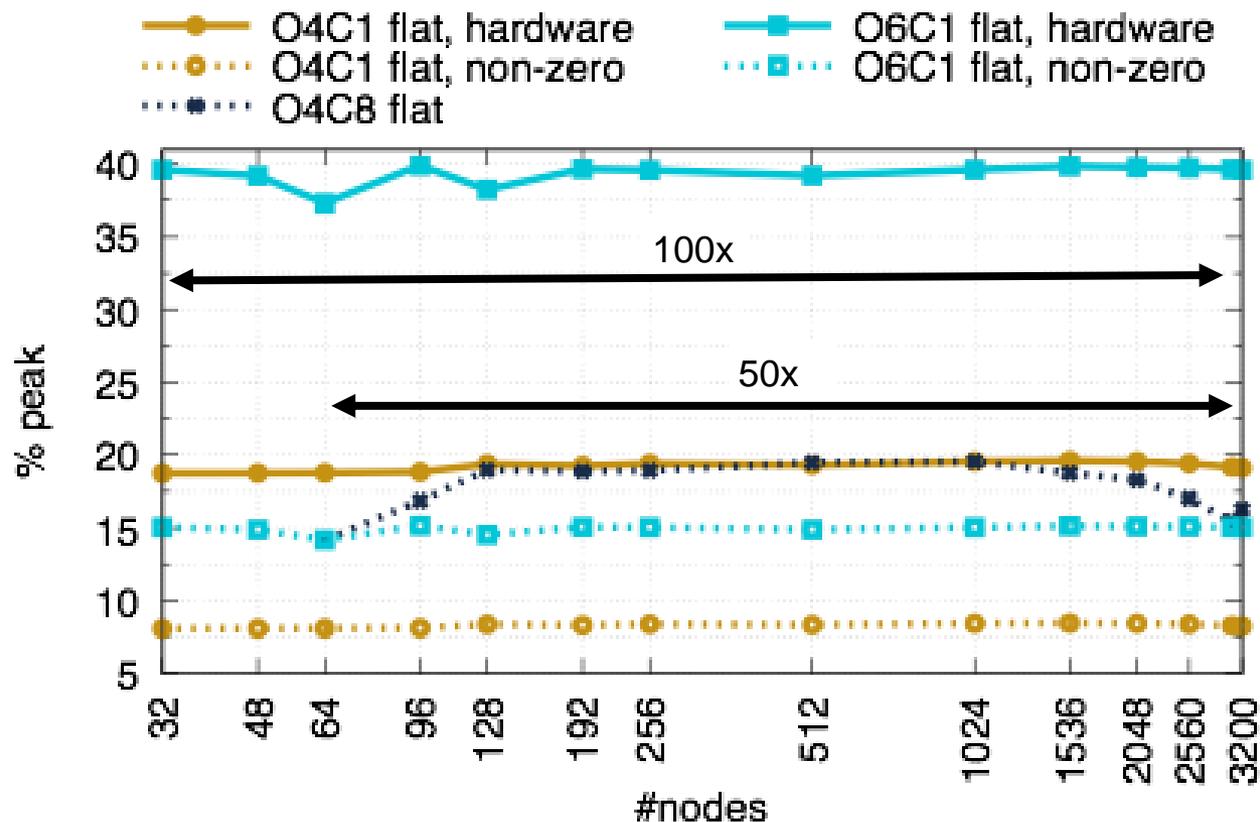
Unstructured tetrahedral  
mesh: 172,386,915  
elements

32-3200 nodes of Theta  
(64 core Intel Xeon Phi  
x200,  
code-named Knights  
Landing)

3200 nodes = 204,800  
cores

O6C1 @ 3.2K nodes: 3.4  
PFLOPS (40% of peak)

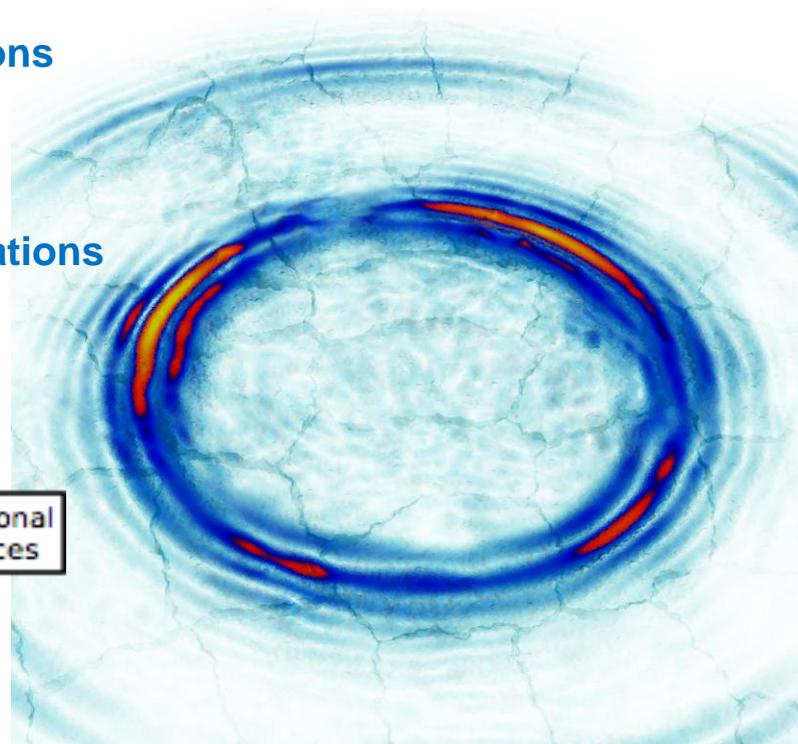
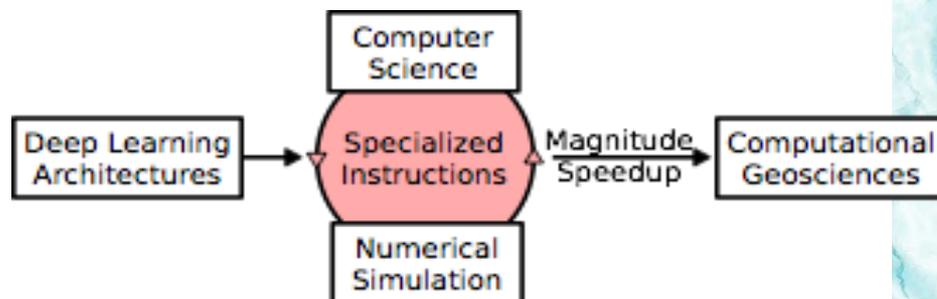
O4C8 vs. O4C1 @ 3.2K  
nodes:  
2.0x speedup



Strong scaling study on Theta. Shown are hardware and non-zero peak efficiencies in flat mode. O denotes the order and C the number of fused simulations [ISC17\_1].

# Outlook: AI Revolution

- **EDGE is a prime candidate for merging traditional HPC and AI**
- **Work in progress: LIBXSMM for AVX512\_4FMAPS (Knights Mill)**
- **Future work: AVX512\_4VNNIW for seismic simulations (Knights Mill)**
- **Future work: Fused simulations to address high-dimensional parameter spaces (“crunching data”):**
  - **EDGElearn: (Deep) Learning from seismic simulations**
- **Future work: LIBXSMM in TensorFlow**



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