#### Marconi cluster @Cineca



#### IXPUG "Birds of a Feather" at ISC

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# Cineca in a nutshell

Cineca is a no-profit consortium composed by 70 italian universities, research institutions and the ministry of research.

- Cineca provides IT services and it is the largest italian supercomputing facility
- Cineca headquarters are in Bologna (selected for the new ECMWF datacenter) and it has offices in Rome and Milan.





# SCAI department at Cineca



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# **SCAI** mission

To support Italian researchers to face global scientific challenges





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# The Cineca ecosystem

- Cineca acts as a hub for innovation and research contributing to many scientifical and R&D projects on italian and european basis.
- In particular, Cineca is a PRACE hosting member and a member of EUDAT.







# MARCONI

Marconi is the new Tier-0 system that replaced the FERMI BG/Q.

- Marconi is planned in two technological stages in a 5 years programme with the objective to reach a 50 Pflop/s system by the year 2019-2020.
- Marconi is a Lenovo NextScale system equipped with Intel Xeon and Intel Xeon Phi processors with an Intel OmniPath network.
- The first stage of MARCONI is made of 3 different partitions (A1, A2 and A3) whose installation started in 2016.
- Marconi is part of the infrastructure provided by Cineca to the EUROFUSION project



# MARCONI A1 : Intel Broadwell

- Started in april 2016 and opened to the production in july 2016
- 1512 compute nodes
- 2 sockets E-2697v4 (18 cores) @2.30 GHz
- 128GB RAM per node
- TPP: 2 PFlop/s





# MARCONI A2: Intel KNL

- Opened to production at the end of 2016
- 3600 compute nodes
- Intel Xeon Phi 7250 (68 cores) @1.40 GHz
- 128GB RAM per node
- Default configuration: Cache/Quadrant
- TPP: 11 PFlop/s





#### First numbers on Marconi KNL







# MARCONI's evolution

In 2017 MARCONI will evolve with the installation of the A3 partition and the final configuration will have:

3024 Intel Skylake nodes (approx. 120960 cores)

- 3600 Intel Knights Landing (approx. 244800 cores)
- Peak performance: about 20 PFlop/s
- Internal network: Intel OPA

In 2019 we expect the convergence of the HPDA infrastructure and the HPC infrastructure towards the target of 50 PFlop/s



# Thanks for your attention



You can download the Cineca annual report 2016 from: https://goo.gl/0zSwQ9



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