A Birds-Eye View of Memory and Cluster Modes on Intel® Xeon Phi™ Processors

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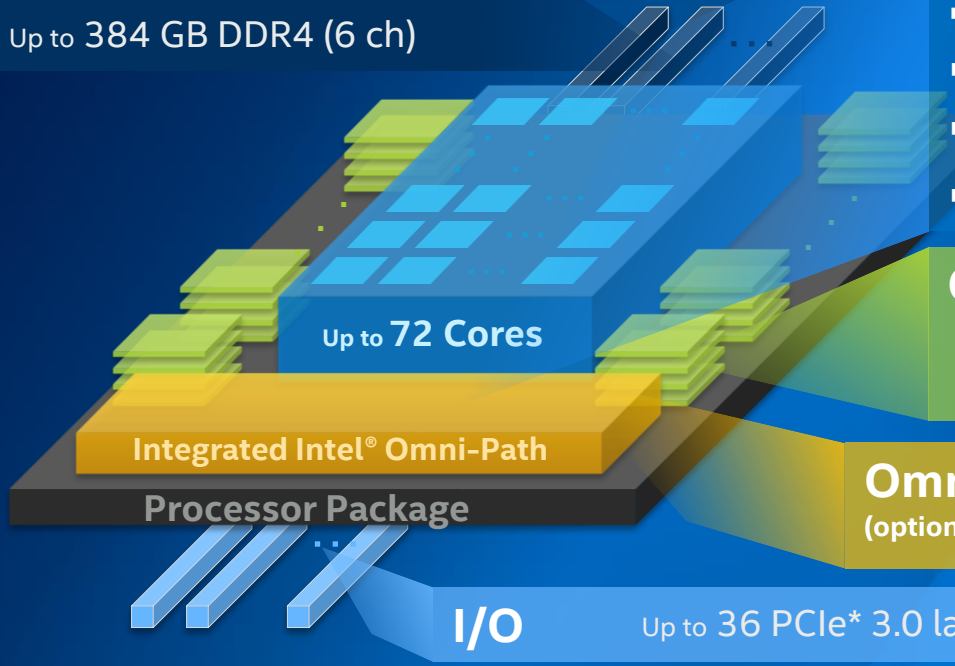
Intel Corporation
IXPUG Birds of a Feather at SC16

Knights Landing

Holistic Approach to Real Application Breakthroughs



Platform Memory

Up to 384 GB DDR4 (6 ch)

Compute

- Intel® Xeon® Processor Binary-Compatible[1]
- **3+ TFLOP/S**[2]
- 2D Mesh Architecture
- Out-of-Order Cores

On-Package Memory

- Over 5x STREAM Triad bandwidth vs. DDR4[3]
- Up to **16 GB** capacity at launch

Omni-Path (optional)

- 1st Intel processor to integrate

I/O

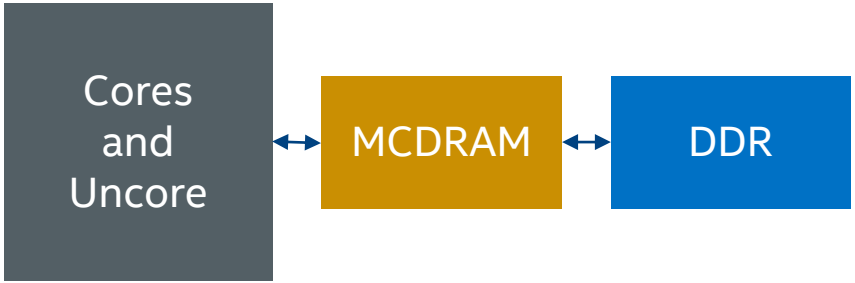
Up to 36 PCIe* 3.0 lanes

1 Binary-Compatible with Intel Xeon processors using Haswell Instruction Set (except TSX).
2 Based on calculated theoretical peak double precision performance capability for a single Intel® Xeon Phi™ Processor 7250: 2 instructions/cycle * 2 floating-point operations (FMA) * 8-wide SIMD * 68 cores * 1.4 GHz = 3.046 TFLOP/s.
3 Based on STREAM benchmark results for Intel Xeon Phi Processor 7250: https://software.intel.com/en-us/articles/optimizing-memory-bandwidth-in-knights-landing-on-stream-triad
* Other names and brands may be claimed as the property of others.

Memory Modes

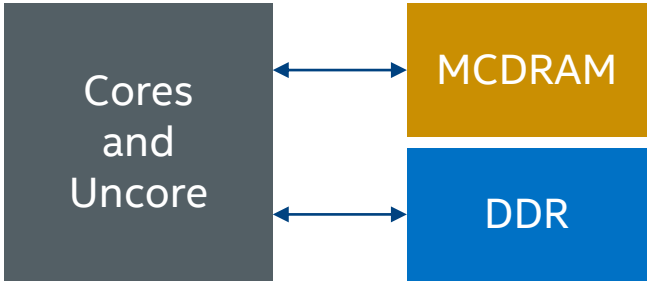
Cache

- Direct-mapped cache.
- Misses are expensive (higher latency) because they access MCDRAM and DDR.
- No source changes required.



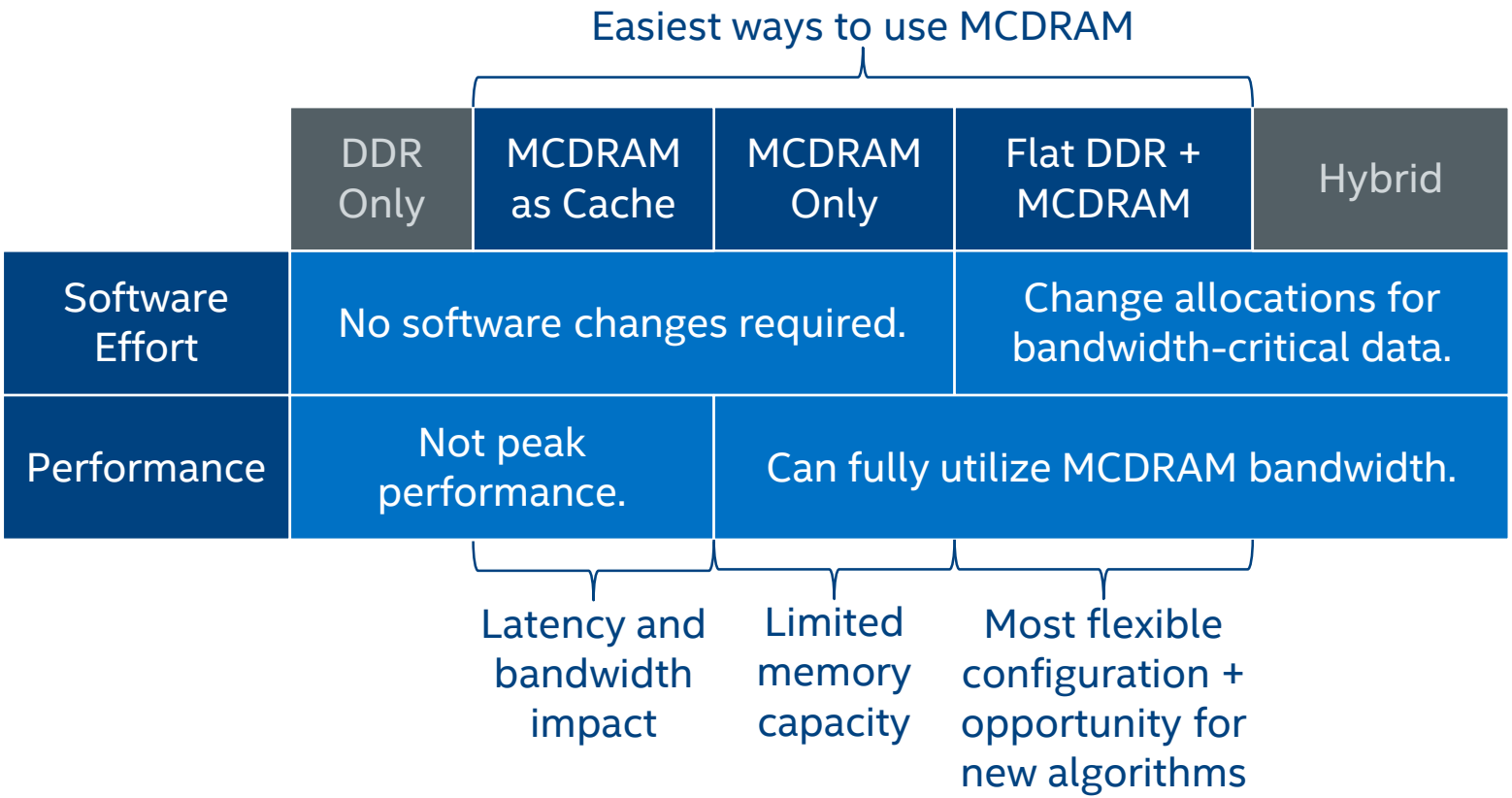
Flat

- Physical address space.
- Exposed as NUMA node(s).
  - `numactl -h`, `lscpu` to display configuration.
- Accessed through libraries/`numactl`.

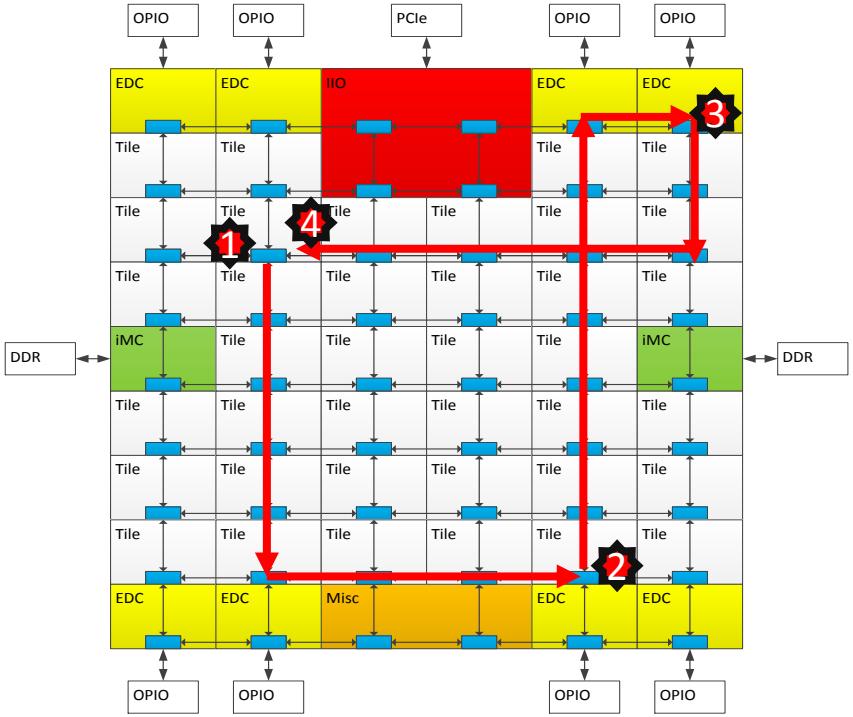


Hybrid mode combines the above in 50% / 50% and 25% / 75% configurations.

Memory Modes: Which to Choose?



Cluster Modes: All-to-All (All2All)



Address Hash:
Uniform across all directories.

Affinity:
No affinity between tile, directory and memory.

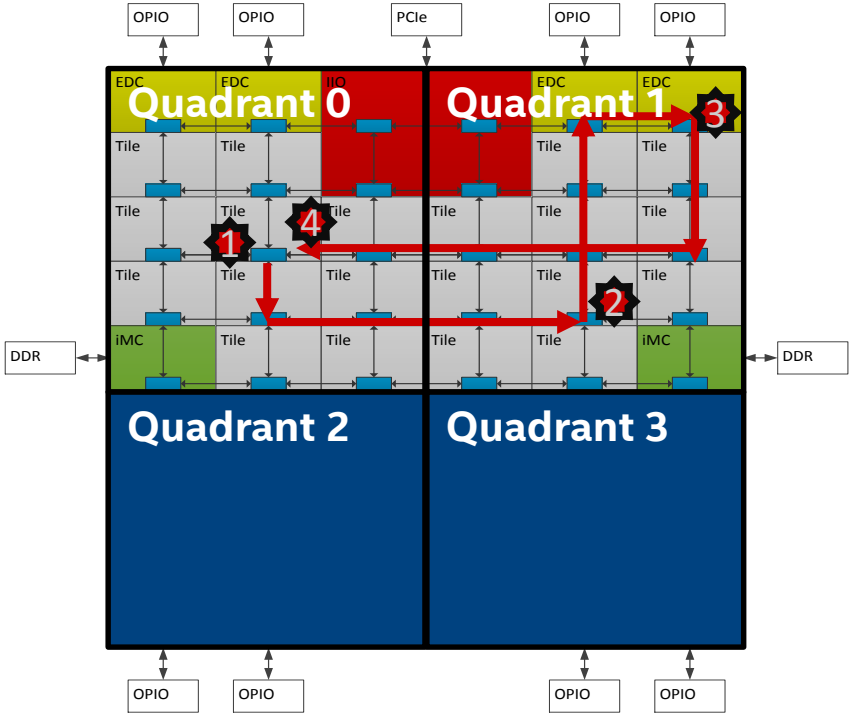
Performance:
Lower than other modes.

Software Changes:
None.

Usage Scenario:
Fallback mode when DDR is unevenly populated.

1. L2 miss; 2. Directory access; 3. Memory access; 4. Data return

Cluster Modes: Quadrant (Quad)



Address Hash:
By quadrant.

Affinity:
Directory and memory in same quadrant.

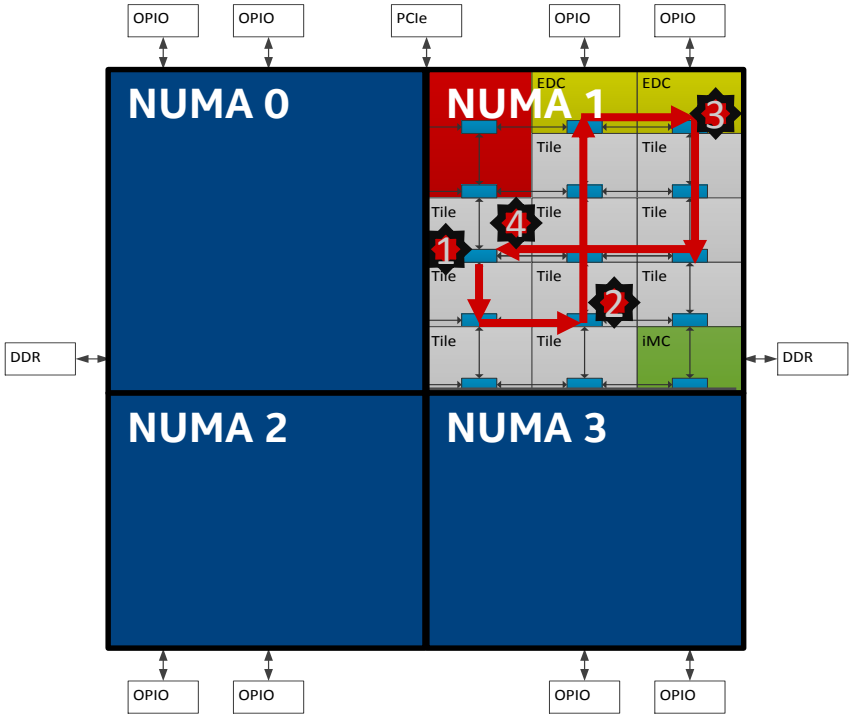
Performance:
Lower latency and higher bandwidth than All2All.

Software Changes:
None.

Usage Scenario:
Default.

1. L2 miss; 2. Directory access; 3. Memory access; 4. Data return

Cluster Modes: Sub-NUMA Clustering (SNC)-4



Address Hash:
By quadrant.

Affinity:
Tile, directory and memory in same quadrant.

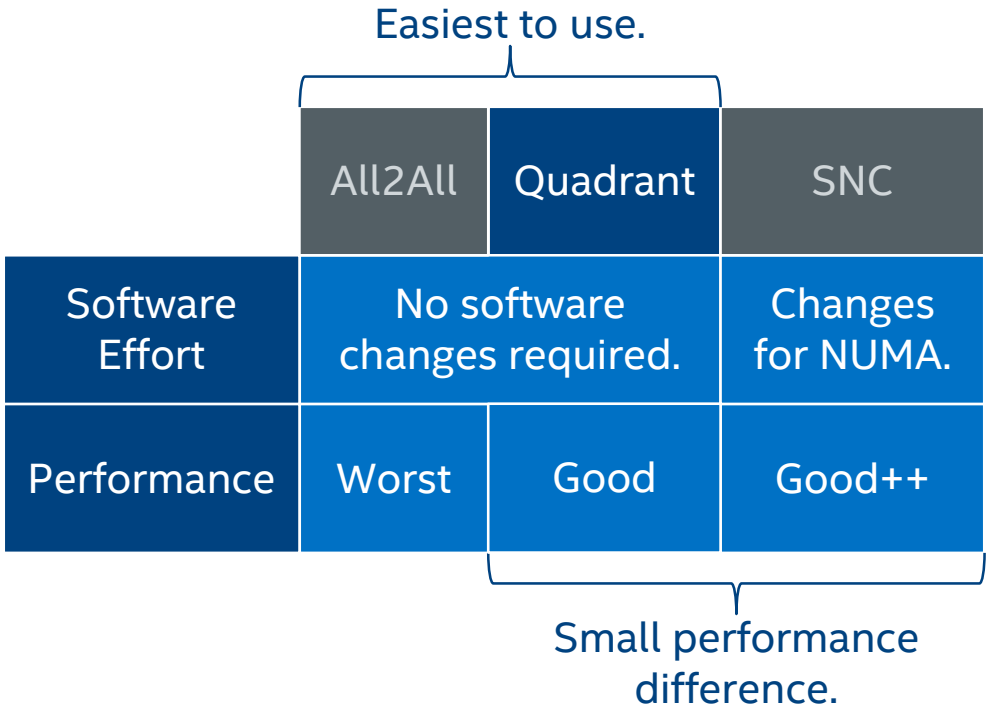
Performance:
Lowest latency of all modes.

Software Changes:
Application/environment must be NUMA-aware.

Usage Scenario:
NUMA-optimized codes or multiple MPI ranks.

1. L2 miss; 2. Directory access; 3. Memory access; 4. Data return

Cluster Modes: Which to Choose?



Summary

- Knights Landing has a lot of possible configurations
  - {Flat, Cache, Hybrid} x {All2All, Hemisphere, Quad, SNC-2, SNC-4}
  - Impact of each upon performance will be application-specific

- Solution: engage with the IXPUG community!
  - Learn from experiences with similar codes
  - Get help with performance analysis/debugging
  - Share ideas/source code/libraries for MCDRAM usage

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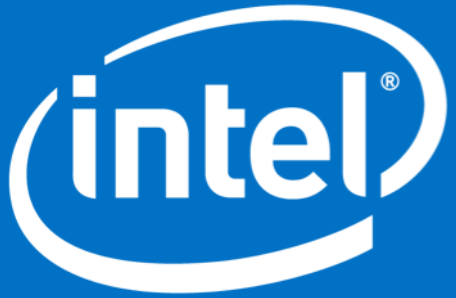
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