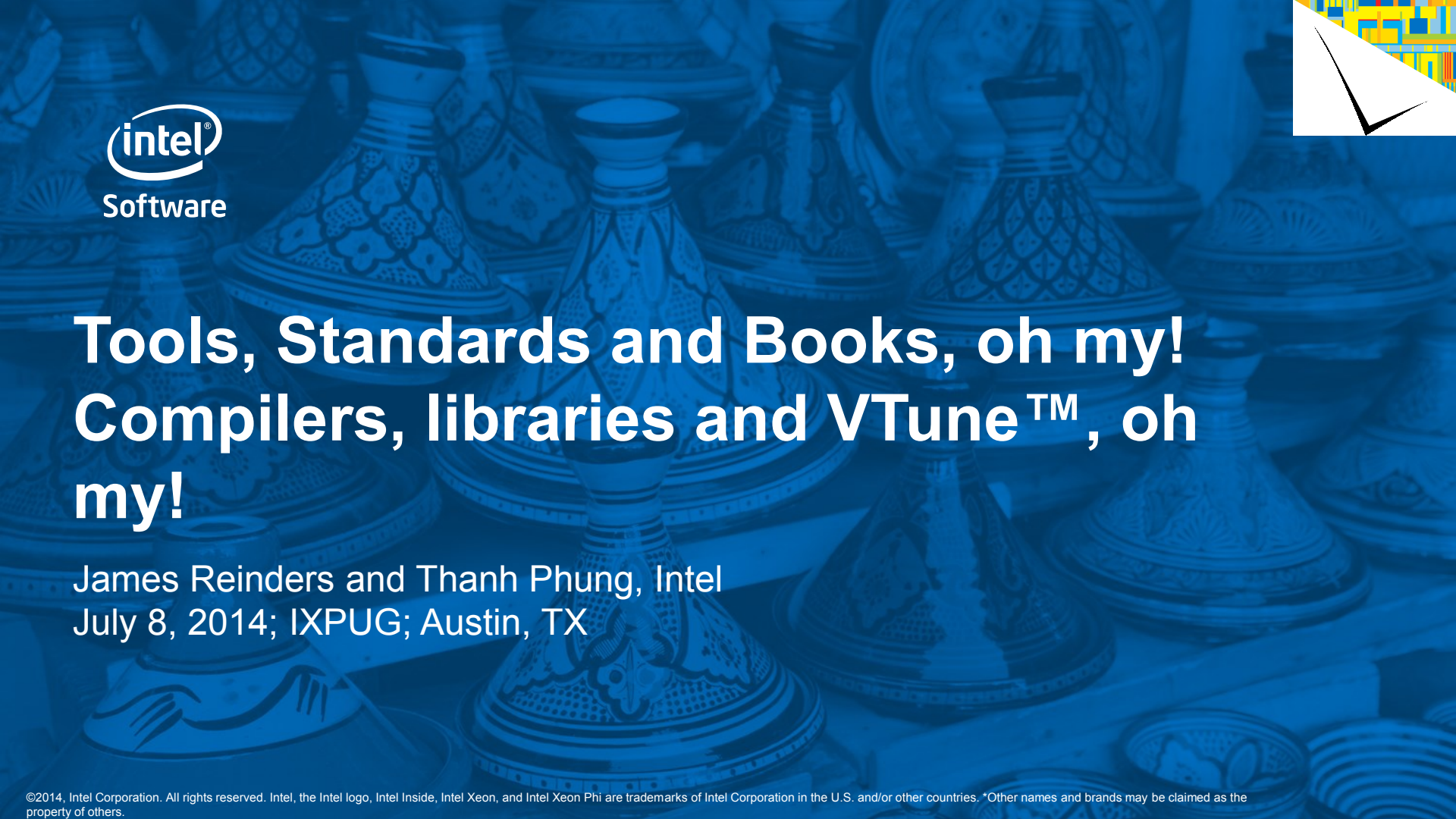


Tools, Standards and Books, oh my! Compilers, libraries and VTune™, oh my!

James Reinders and Thanh Phung, Intel
July 8, 2014; IXPUG; Austin, TX

Thank you for being a part of this Intel® Xeon Phi™ Users Group.

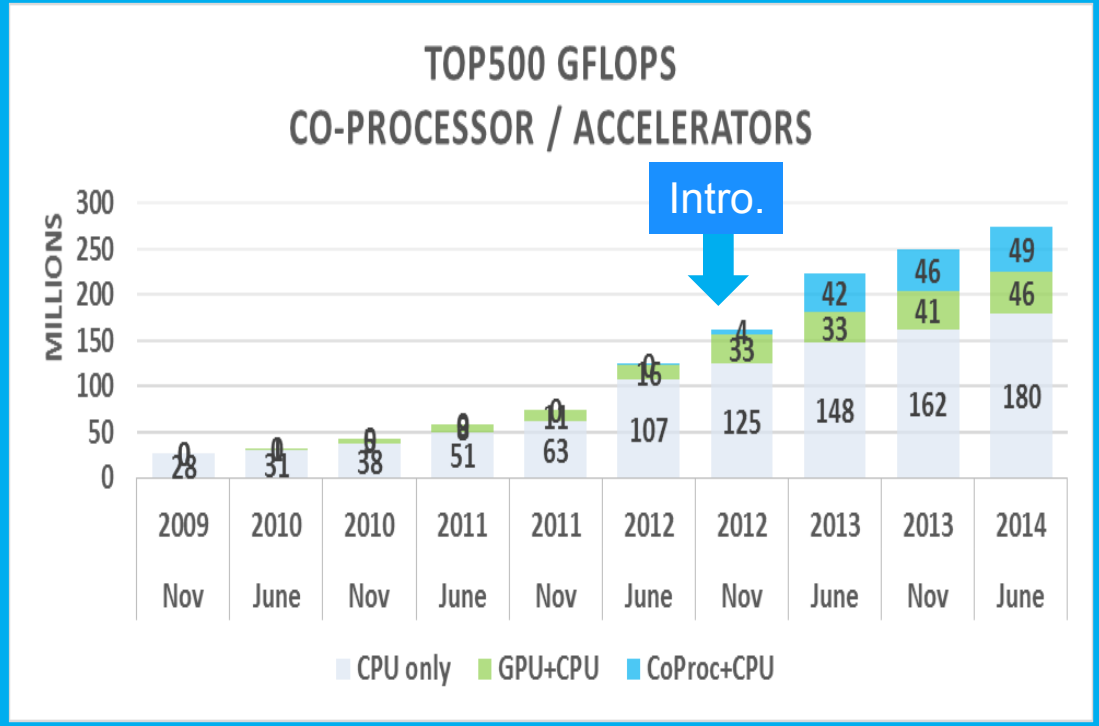
Neo-Heterogeneous Computing

The "promise" of heterogeneous systems
but with a homogeneous programming environment.

It's a lot more to us than a cute marketing phrase.
It started as a technical concept, and remains one for us *all*.

It’s the Programming Model, Stupid.

June 2014 Top 500 List



#1 system
(third time)

Neo-heterogeneous

(Intel® Xeon® Processors +
Intel® Xeon Phi™ Coprocessor)

Common
Programming
Model

Source: www.top500.org

Investing forward

- Knights Landing
- Programming Standards and their growth/evolution
- Intel Parallel Computing Centers (IPCCs)
- Education: course work

Knights Landing

(Next Generation Intel® Xeon Phi™ Products)

Continued programming model advantag
Add Intel® AVX-512 instructions
gcc work well underway

Platform Memory: DDR4 Bandwidth and Capacity Comparable to Intel® Xeon® Processors

Conceptual—Not Actual Package Layout

Compute: Energy-efficient IA cores

- *Microarchitecture enhanced for HPC*
- ***3X** Single Thread Performance vs Knights Corner*
- *Intel Xeon Processor Binary Compatible*

On-Package Memory:

- *up to **16GB** at launch*
- ***1/3X** the Space*
- ***5X** Bandwidth vs DDR4*
- ***5X** Power Efficiency*

Jointly Developed with Micron Technology

3+ TFLOPS
In One Package
Parallel Performance & Density

2nd half '15
1st commercial systems

Investing forward

- Knights Landing
- Programming Standards and their growth/evolution
- Intel Parallel Computing C
- Education: course work

Latest Intel tools in beta (2015)
OpenMP* 4.0 support
Explicit Vectorization
(see my SGIUG talk – lotsofcores.com)
A talk about the need for explicit vectorization, given at SGIUG on April 30, 2014

Investing forward

- Knights Landing
- Programming Standards and their growth/evolution
- Intel Parallel Computing Centers (IPCCs)
- Education: course work

AMBER WRF VISIT VASP UTBENCH SU2 SG++ SeisSol, GADGET, SG++ ROTOR SIM R Quantum Espresso Optimized integral OPENMP/ MPI Openflow NWChem

AVBP (Large Eddy) NEMO5

Announcing new mailing list: **http://tinyurl.com/IPCCmaillist**

New IPCCs being added (rolling basis)

Watch for University of Oregon developed 4/500 level curriculum

MPAS

Blast

Intel® Parallel Computing Centers

Mardyn

BUDE

MACPO

CAM-5

Ls1

CASTEP

Harmonie

Castep

GTC

CESM

GS2

CFSv2

Gromacs

CIRCAC

GPAW

CliPhi (COSMOS) COSA Cosmos codes DL-MESO DL-Poly ECHAM6 Elmer FrontFlow/Blue Code GADGET GAMESS-US

*Other brands and names are the property of their respective owners.

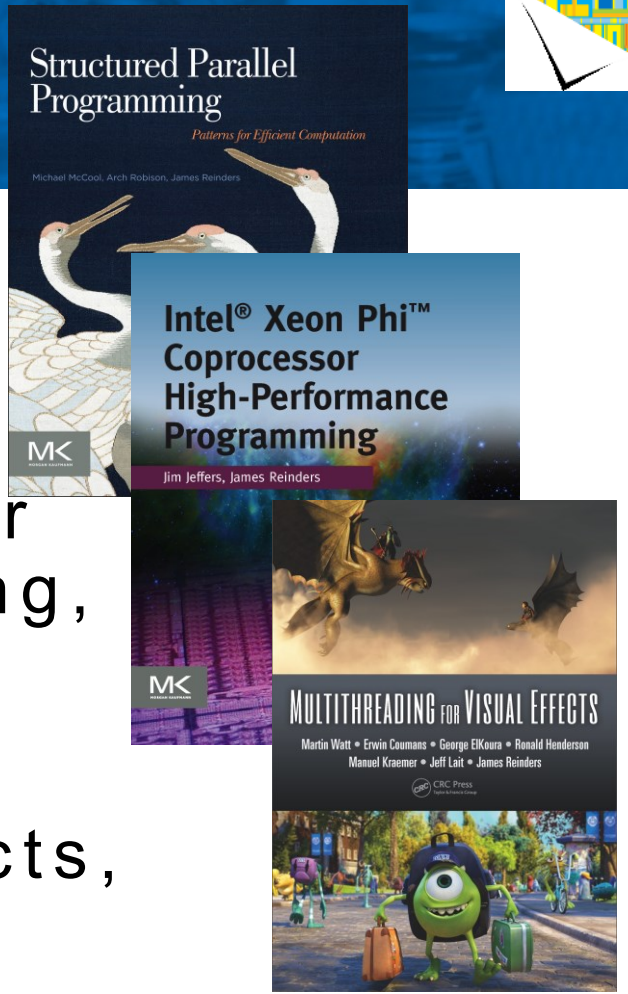
Investing forward

- Knights Landing
- Programming Standards and their growth/evolution
- Intel Parallel Computing Centers (IPCCs)
- Education: course work

Structured Parallel Programming, 2012

Intel® Xeon Phi™ Coprocessor High-Performance Programming, 2013

Multithreading for Visual Effects, 2014 *(June)*



User driven – contribution based books on parallel programming – "inspired by the highly scalable Intel® Xeon Phi™ Coprocessor"

High Performance Parallelism Pearls – Successful Approaches for Multicore and Many-core Programming

http://lotsofcores.com/gems

Status:

- Volume 1 – **DEFINITELY HAPPENING**
  being written/edited, target availability end of 2014
- Volume 2 – **PLANNED** ***(assume volume 1 is a "hit")***
  submissions being accepted (writing due end of 2014), publish in 2015

submit your proposal now: http://lotsofcores.com/gems

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james.r.reinders@intel.com

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Notice revision #20110804