DM-HEOM:

A Portable and Scalable Solver-Framework for the Hierarchical Equations of Motion

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Zuse Institute Berlin Distributed Algorithms and Supercomputing

Observations:

- many HPC applications are legacy code
 - $\Rightarrow\,$ written and incrementally improved

by domain scientists

 \Rightarrow often without (modern) software engineering



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- software life time: multiple tens of years \Rightarrow outlives systems by far
- \Rightarrow need for code modernisation

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- modern methods and technologies with a community beyond HPC

Contributions

a) 1st Distributed Memory implementation of the HEOM method: DM-HEOM

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b) Interdisciplinary development workflow

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b) Interdisciplinary development workflow

c) Design guidelines/experiences for performance portable HPC applications

- understand the energy transfer in photo-active molecular complexes
 - \Rightarrow e.g. photosynthesis
 - ... but also quantum computing



[Image by University of Copenhagen Biology Department]

- understand the energy transfer in photo-active molecular complexes
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- millions of coupled ODEs

$$\begin{aligned} \frac{d\sigma_u}{dt} &= -\frac{i}{\hbar} [H, \sigma_u] \\ &- \sigma_u \sum_{b=1}^B \sum_k^{K-1} n_{u,(b,k)} \gamma(b,k) \\ &- \sum_{b=1}^B \left[\frac{2\lambda_b}{\beta \hbar^2 \nu_b} - \sum_k^{K-1} \frac{c(b,k)}{\hbar \gamma(b,k)} \right] V_{s(b)}^{\times} V_{s(b)}^{\times} \sigma_u \\ &+ \sum_{b=1}^B \sum_k^{K-1} i V_{s(b)}^{\times} \sigma_{u,b,k}^+ \\ &+ \sum_{b=1}^B \sum_k^{K-1} n_{u,(b,k)} \theta_{MA(b,k)} \sigma_{(u,b,k)}^- \end{aligned}$$

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$\frac{\mathrm{d}\sigma_{\mathrm{u}}}{\mathrm{d}\mathrm{t}} = -\frac{\mathrm{i}}{\hbar} \left[H, \sigma_{u}\right]$	(LvN commutator)
+ $\sum_{\text{baths}} A\sigma_u$	(same node)
+ $\sum_{\text{baths}} B\sigma_{u_+}$	(links to layer+1)
+ $\sum_{\text{baths}} C \sigma_{u_{-}}$	(links to layer-1)

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- millions of coupled ODEs
- hierarchical graph of complex matrices (auxiliary density operators, ADOs)
 - \Rightarrow dim: $N_{\rm sites} \times N_{\rm sites}$
 - \Rightarrow count: exp. in hierarchy depth d





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	compute	memory bw.	
Device Name (architecture)	[TFLOPS]	[GiB/s]	[FLOP/Byte]
$2 \times$ Intel Xeon Gold 6138 (SKL)	2.56	238	10.8
$2 \times$ Intel Xeon E5-2680v3 (HSW)	0.96	136	7.1
Intel Xeon Phi 7250 (KNL)	2.61^{a}	$490/115^{ m b}$	5.3/22.7 ^b
Nvidia Tesla K40 (Kepler)	1.31	480	2.7
AMD Firepro W8100 (Hawaii)	2.1	320	6.6

^aAssuming 1.2 GHz AVX frequency. ^bOn-chip MCDRAM / DRAM

HEOM - Example Systems

system		baths	depth	total
name	$N_{\rm sites}$	per site	d	ADO memory
FMO	7	22	8	2.8 GiB
LHC II monomer	14	1	3	5.6 GiB
PS I	96	1	3	129.2 GiB
PS I	96	1	4	3231.0 GiB

memory consumption assuming an RK4 solver

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 - time to solution
- $\Rightarrow\,$ distributed memory implementation required







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- PDEs
- Graphs
- . . .





computer scientists



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High-Level Prototype (Mathematica)

- domain scientist's tool
- high level
- symbolic solvers
- arbitrary precision
- very limited performance

Mathematical Model

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OpenCL (Open Computing Language) in a Nutshell

- open, royalty-free standard for cross-platform, parallel programming
- maintained by Khronos Group

- personal computers, servers, mobile devices and embedded platforms
- first released: 2009-08-28

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OpenCL Platform and Memory Model



OpenCL Platform and Memory Model



Memory Model:

- CD has device memory with glottal/constant addr. space
- CU has local memory addr. space
- PE has private memory addr. space
- \Rightarrow relaxed consistency

OpenCL Platform	CPU Hardware	GPU Hardware
Compute Device	Processor/Board	GPU device
Compute Unit	Core (thread)	Streaming MP
Processing Element	SIMD Lane	CUDA Core
global/const. memory	DRAM	DRAM
local memory	DRAM	Shared Memory
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- \Rightarrow write code for this **abstract machine model**
- \Rightarrow device-specific OpenCL compiler and runtime maps it to actual hardware

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- \Rightarrow currently: widest practical portability of parallel programming models

Interdisciplinary Workflow

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- separation and exchangeability of different aspects and strategies
 - partitioning, numerical methods, memory layout, parallelisation, communication, etc.

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C++ App. with OpenCL kernel

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 - \Rightarrow encapsulates OpenCL kernel code
- OpenCL Config specifies runtime configuration
- Solver works on ODE
 - \Rightarrow encapsulates OpenCL runtime
 - \Rightarrow encapsulates numerics
 - \Rightarrow produces *Results*

From Portability to Performance

OpenCL:

- guarantees portability . . .
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Strategy:

- 1. identify key optimisations each device requires
- 2. make the code configurable to the device's needs
 - ... without writing a version for each device

Performance Portability: Node-Level OpenCL Runtime Kernel Compilation

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 - a) facilitate compiler optimisation
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a) compiler optimisation:

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 - e.g. sizes, loop-counts, ...
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b) configurable kernel code:

- work-item granularity
- memory-layout

Runtime compilation for non-OpenCL codes: https://github.com/noma/kart

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- \Rightarrow one ADO matrix element per thread

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⇒ requires a **compile-time configurable outer loop-nest** inside the kernel

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\Rightarrow match requirement of device-specific memory architecture

- GPU: coalesced access from working-groups without bank-conflicts
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- CPU: contiguous SIMD vector load/store instructions (avoid gather/scatter ops)
- \Rightarrow parallelisation strategy, granularity and memory layout must match
 - e.g. outer loop vectorisation for SIMD architectures





work-item ₁ work-item ₂ work-item ₃		work-item $_8$	\Rightarrow mapped to 8 SIMD lanes
--	--	----------------	--------------------------------------







Interdisciplinary Workflow

domain experts

Mathematical Model

- ODEs
- PDEs
- Graphs

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- domain scientist's tool
- high level
- symbolic solvers
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- replace some code with OpenCL
- compare results
- figure out numerics
- use accelerators in MM



- start single node
- OpenCL 1.2 for hotspots
- modern C++ 11/14/17
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C++ App. with OpenCL kernel Distributed Application (MPI)

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- scale to multiple nodes
- partitioning,
 - neighbour exchange, ...
- wrapped MPI 3.0

Partitioning the Hierarchy

- **Problem**: map hierarchy graph nodes to *n* partitions (compute nodes)
 - minimise communication
 - minimise load imbalance
- \Rightarrow GP is **NP-hard**
- $\Rightarrow\,$ hierarchy graph is highly connected
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part-	neighbor parts.			hierarchy nodes per part. (avg)			
itions	avg	min	max	nodes	shared %	halo	overhead %
16	15	15	15	9803	91.7%	12508	127.6%
32	31	31	31	4902	95.0%	7858	160.3%
64	62	60	63	2451	96.8 %	4739	193.2%
128	127	125	127	1225	98.0 %	2958	241.4 %
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 \Rightarrow highly connected partitioning graph \Rightarrow almost **all-to-all**

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 \Rightarrow almost all nodes required by other partitions

 \Rightarrow prevents inner/outer communication/computation overlap

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 \Rightarrow more halo nodes than local nodes





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 - Derived Data Types
 - \Rightarrow fully **declarative** communication API
- ODE can trigger action
 - $\Rightarrow\,$ neighbor exchange prior to evaluation

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- always collect perf. data
- profile/tune code
- explore new architectures

Benchmarks: Work-item Granularity



Impact of Work-item Granularity

Benchmarks: Work-item Granularity



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Benchmarks: Memory Layout



Impact of Configurable Memory Layout

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Performance Portability Relative to Xeon (SKL)



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Performance Portability Relative to Xeon (SKL)

 \Rightarrow gray bars are expected runtimes extrapolated from peak FLOPS



Performance Portability Relative to Xeon (SKL)

 \Rightarrow Older Haswell Xeon exceeds expectations, due to better OpenCL support



Performance Portability Relative to Xeon (SKL)



Performance Portability Relative to Xeon (SKL)

 \Rightarrow KNL and K40 sensitive to irregular accesses from extreme coupling in this scenario.

Strong Scaling of PS I with 3 Layers



Strong Scaling of PS I with 3 Layers





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Strong Scaling of PS I with 3 Layers



👄 communication 📥 compute 📥 sum

Strong Scaling of PS I with 3 Layers



Summary

Lessons's learned:

- interdisciplinary workflow is key for developing HPC codes
- standards (OpenCL, MPI-3, ...) enable portability
- a *flexible* design enables **portable performance**
 - \Rightarrow leverage runtime compilation
 - \Rightarrow work-item granularity and memory and layout



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DM-HEOM:

- first Distributed Memory HEOM implementation
- pushes the boundary of feasible problem sizes
- practical scalability from laptops to supercomputers

Thank you.

Feedback? Questions? Ideas?

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